SmartAMC™

AMC'97 Audio Modem Codec with Audio Codec and Host-Processed V.90/K56flex™ Modem using CX20468 Host Side Device and CX20463 SmartDAA™ for AC-link (AC'97 2.1) Applications

Data Sheet

Conexant Proprietary Information

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CONEXANT™

Revision Record

Revision	Date	Comments
A	7/18/2000	Initial release.

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1 Introduction

1.1 Overview

The Conexant™ SmartAMC™ Audio Modem Codec (AMC) is compliant with Intel Audio Codec ’97 2.1 Extensions for a combo audio modem codec (AMC’97). The modem supports V.90 analog data up to 56 kbps, V.17 analog fax to 14.4 kbps, voice/telephone answering machine (TAM), and high quality soft speakerphone. The modem operates with PSTN telephone lines in the U.S. and world-wide. The SmartAMC is also supplied with either basic or enhanced audio software. Table 1-1 lists the available models.

The SmartAMC™ AMC with AC-link interface supports Communication and Networking Riser (CNR), Advanced Network Riser (ACR), Audio/Modem Riser (AMR), Mobile Daughter Card (MDC), and Mini PCI interfaces for applications such as embedded/plug-in modems.

Conexant's SmartDAA™ technology (patent pending) eliminates the need for a costly line transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations. The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling world-wide homologation of a single modem board design.

The SmartDAA system side powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant’s proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost for world-wide support.

For over a decade, Conexant has assisted customers with DAA technology and homologation. This expertise and system level approach has been leveraged in this product.

The SmartAMC device set, consisting of an CX20468 Host Side Device (HSD) in a 48-pin TQFP and a CX20463 SmartDAA Line Side Device (LSD) in a 32-pin TQFP, supports data/fax/voice/TAM and DAA (Digital Access Arrangement)/telephone line interface functions (Figure 1-1). Figure 1-2 identifies the major hardware signal interfaces. Figure 1-3 identifies typical supported MC configurations.

A simplified block diagram of the SmartAMC audio codec is shown in Figure 1-4.

Audio recording and playback over the telephone line interface using A-Law, μ-Law, or linear coding at 8 kHz sample rate supports applications such as remote digital telephone answering machine (TAM).

The SmartAMC can operate with Conexant-qualified AC’97-compliant core logic chip sets.

1.2 Distinguishing Features

- V.90 data/V.17 fax soft modem, MMX optimized
- SmartDAA technology
  - Eliminates many costly traditional DAA discrete components
  - Reduces modem and DAA board footprint
  - Allows a single modem board design to be approved for world-wide shipments
  - Line-in-use detection
  - Remote hangup detection
  - Extension off-hook detection
  - Wake-up on ring for primary/secondary codec
- Telephony/voice/TAM
- Supports selected AC'97-compliant core logic
- Supports soft speakerphone
- Data/Fax/Voice call discrimination
- World-class operation (optional)
- Industry standard communication commands
- AC-link (AC'97 2.1 compatible) host interface
  - Single line Data/Fax/Voice/TAM modem codec
  - Operable as a primary or a secondary codec
  - Supports CNR, ACR, AMR, MDC, and Mini PCI host interface
  - Sleep current less than 1 mA
- System compatibility
  - Windows Driver Model (WDM)
  - Windows 95/98, Windows NT 4.0, Windows 2000, Windows Millennium
  - Microsoft PC 98 and PC 99 compliant
  - Advanced Power Management (APM and ACPI)
- V.80 synchronous access
- Full-duplex modem codec with 16-bit resolution
- +3.3V analog and IO operation
- Extensive audio interface
  - Stereo full-duplex audio codec with 18-bit resolution
  - Four audio analog input channels
  - Two audio analog output channels
  - One audio digital output channel
  - Hardware sample rate converters
  - Multiple audio channels
  - 32 Ω headphone driver

1.3 Applications

- Primary or secondary audio/modem CNR, ACR, AMR, and MDC card
- Speakerphone using HAL based audio/modem driver
- Embedded/plug-in Mini PCI modems

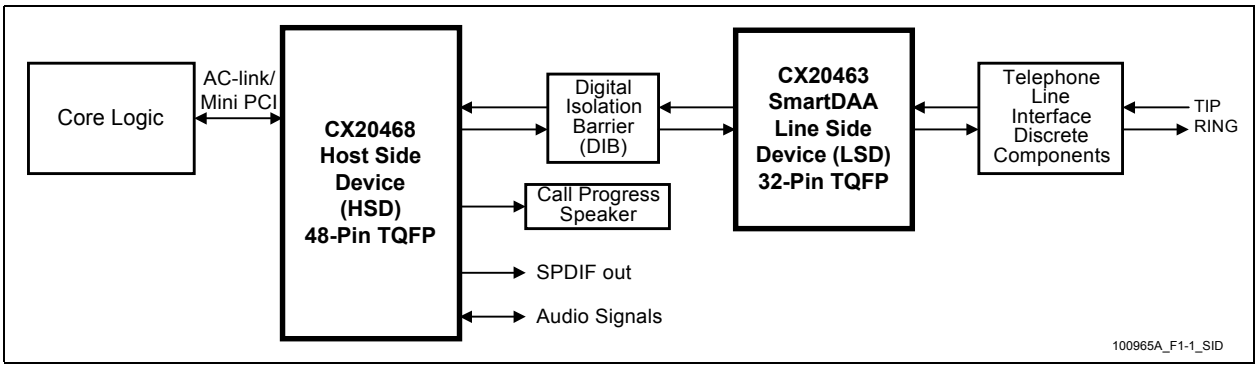

Figure 1-1. SmartAMC Devices and Major Signal Interfaces

Table 1-1. SmartAMC Models and Functions

Model/Order/Part Numbers				Supported Functions				
Marketing No.*	**Device Set Order No.**	**Host Side Device (HSD) [48-Pin TQFP] Part No.**	**SmartDAA Line Side Device (LSD) [32-Pin TQFP] Part No.**	**V.90/K56flex Data, V.17 Fax, Voice/TAM, Worldwide**	**Basic Audio**	**Speakerphone**	**Conexant Player**	**HRTF, EAX**
SmartAMC/W	DSAC-L500-001	CX20468-11	20463-11	Y	Y	—	—	—
SmartAMC/WS	DSAC-L500-011	CX20468-11	20463-11	Y	Y	Y	—	—
SmartAMC/WP	DSAC-L500-021	CX20468-11	20463-11	Y	Y	—	Y	—
SmartAMC/WEHRTF	DSAC-L500-031	CX20468-11	20463-11	Y	Y	—	—	Y
SmartAMC/WMAX	DSAC-L500-041	CX20468-11	20463-11	Y	Y	Y	Y	Y

Notes:
1. Model options:
   - W Worldwide
   - S Basic Audio and Speakerphone
   - E Basic Audio and Conexant Player
   - EHRTF Basic Audio, Head Related Transfer Function (HRTF) and EXA
   - MAX Basic Audio, Speakerphone, Conexant Player, HRTF, and EXA
2. Supported functions (Y = Supported; – = Not supported)
3. For ordering purposes, the CX prefix may not be included in the part number for some devices. Also, the CX prefix may not appear in the part number as branded on some devices.

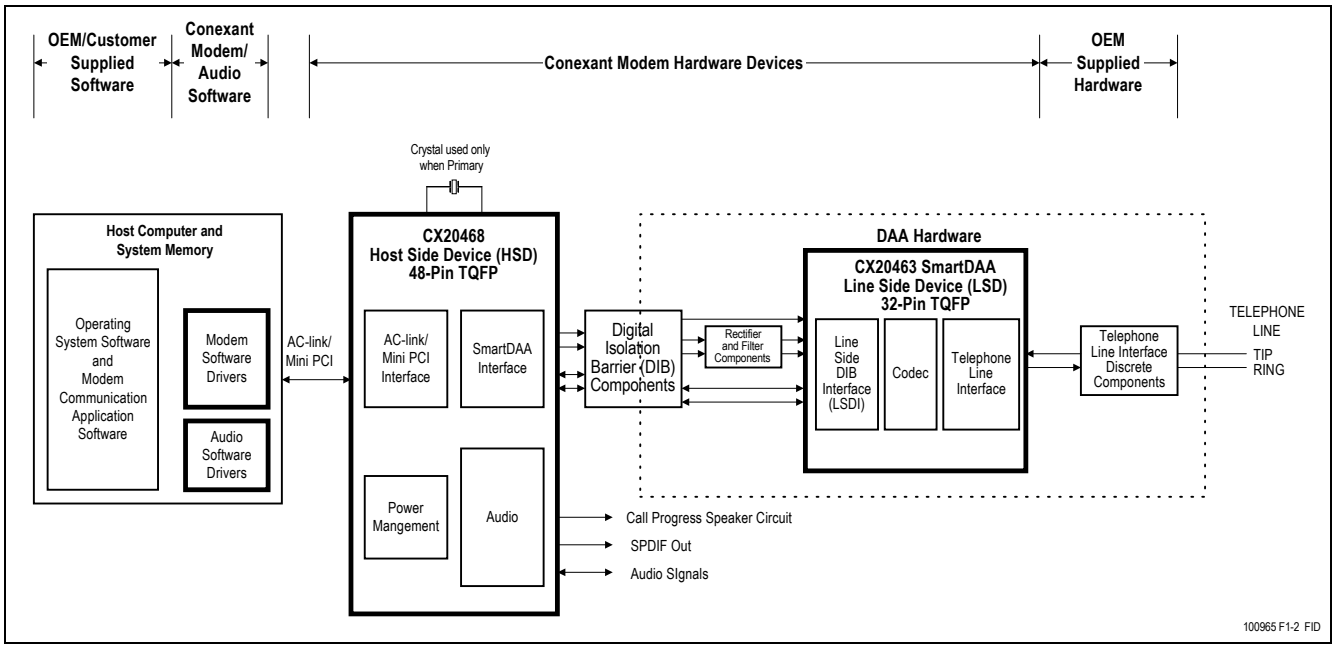

Figure 1-2. SmartAMC Major Interfaces

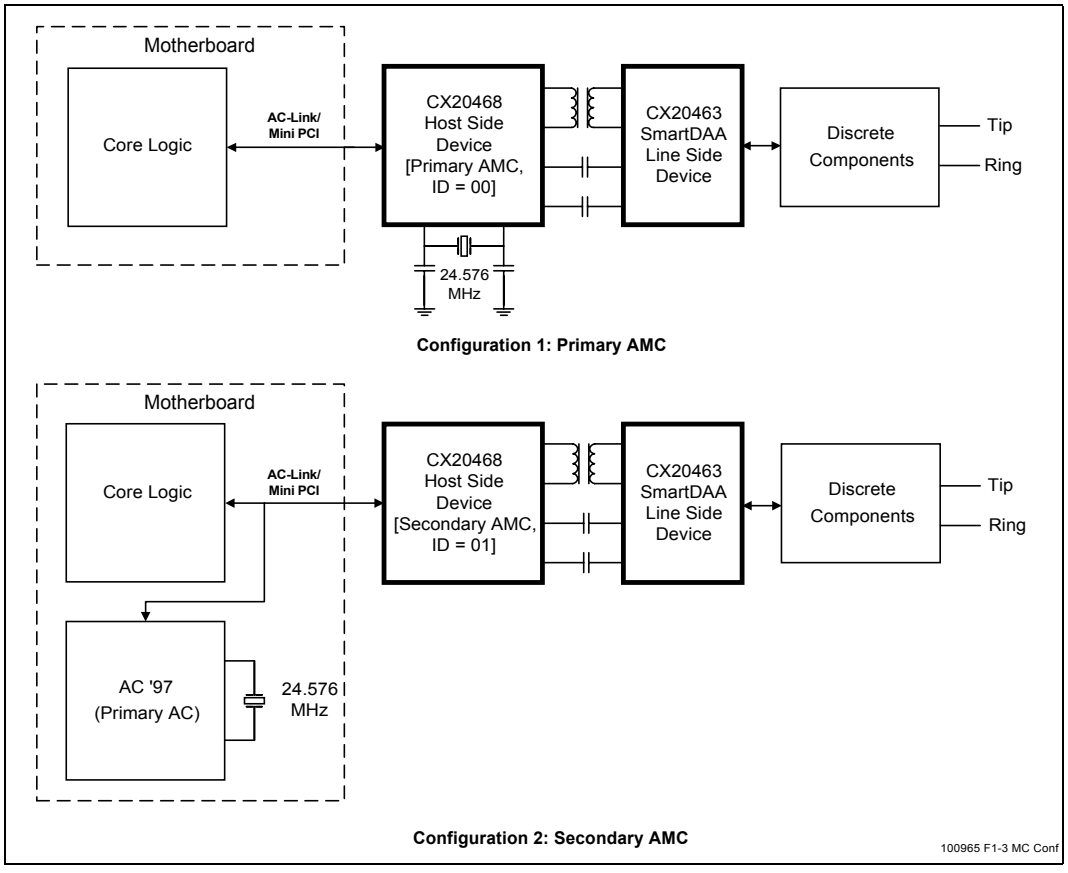

Figure 1-3. Typical Supported AMC Configurations

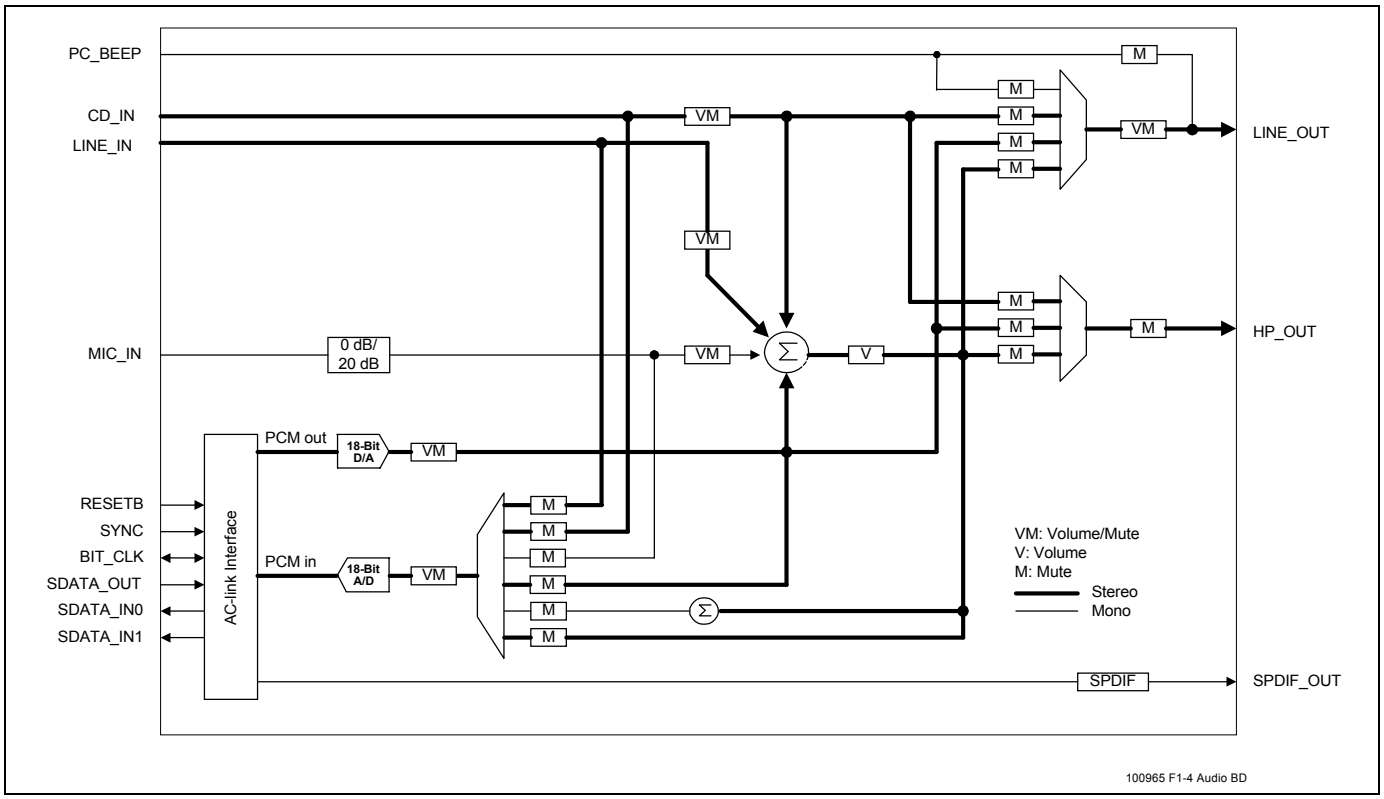

Figure 1-4. SmartAMC Audio Codec Functional Block Diagram

1.4 Detailed Features

1.4.1 General Audio Modem Features

- V.90 data modem with receive rates up to 56 kbps and send rates up to V.34 rates
  - ITU-T V.90, K56flex, V.34 (33.6 kbps), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - V.250 and V.251 commands
- V.17 fax modem with send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 channel 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0 commands
- Telephony/Voice/TAM
  - V.253 commands
  - 8-bit μ-Law/A-Law coding (G.711)
  - 8-bit/16-bit linear coding
  - 8 kHz sample rate
  - Concurrent DTMF detect, ring detect and caller ID
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- V.8/V.8bis and V.251 commands
- Data/Fax/Voice call discrimination
- Host software-based signal processing
- Single configuration profile stored in host
- Worldwide operation
  - Complies to TBR21 and other country requirements
  - Caller ID detection
- System compatibility
  - Windows Driver Model (WDM)
  - Windows 95/98 operating system
  - Windows NT 4.0, Windows 2000, Windows Millennium operating systems
  - Microsoft PC 98 and PC 99 Design Initiative compliant
  - Advanced Power Management (APM and ACPI)
  - Unimodem/V compliant
  - Pentium 166 MMX MHz-compatible or greater
  - 32 Mbyte RAM or more
- Sony Philips Digital Interface (S/PDIF) output
  - Linear PCM consumer mode
  - AC3-bit stream consumer mode
- Hardware sample rate converters
  - High performance: 48 kHz and 44.1 kHz
- Four audio analog input channels
  - MIC_IN, LINE_IN, CD_IN, and PC_BEEP
- Two audio analog output channels
  - LINE_OUT and HP_OUT
- Multiple audio channels
  - PCM Left and Right as a primary configuration (slots 3 and 4)
  - PCM Left and Right Surround as a secondary (slots 7 and 8)
  - PCM Center and LFE as a secondary (slots 6 and 9)
- 32 Ω headphone driver
- Thin packages support low profile designs (1.6 mm max. height)
  - CX20468 HSD: 48-pin TQFP
  - CX20463 LSD: 32-pin TQFP
- +3.3V operation

1.4.2 AC-link (AC'97) Host Interface Features

- Operates as a single-line Data/Fax/Voice/TAM modem
- AC'97 rev 2.1 compatible codec with the LSD and DIB (uses protocol slot 5 and 12)
- Uses +3.3VSB for power management mode
- Wake-on-ring in primary and secondary codec
- Sleep current: 1 mA typical
- Supports selected AC'97-compliant core logic
- Supports soft speakerphone using HAL based Audio/Modem driver
- Operable as either a primary or a secondary codec selected by external pin configuration.
  - BIT_CLK is the input bit clock in secondary codec operation
  - BIT_CLK is the output bit clock (derived from external crystal) in primary codec operation
- Supports Power Management
  - ACPI Power Management Registers
  - APM support
  - Wake-on ring in D3cold

1.4.3 SmartDAA Features

- System side powered DAA operates under poor line current supply conditions
- Wake-on-ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Pulse dialing
- Line-in-use detection – detects even while on-hook
- Remote hang-up detect – for efficient call termination
- Extension pickup detect
- Handset exclusion (patent pending)
- Call waiting detection
- Digital PBX line protection
- Meets world-wide DC VI Masks requirements

1.5 Reference Design

CNR, ACR, AMR, and MDC reference design cards are available to minimize application design time and costs.

The cards are pretested to pass FCC Part 15, Part 68, and TBR 21.

A design package is available in electronic form for each design. The design package includes schematics, bill of materials (BOM), vendor parts list (VPL), board layout files in Gerber format, and complete documentation.

The reference designs are production ready for immediate manufacturing. The design can also be used for the basis of a custom design by the OEM to accelerate design completion for rapid market entry.

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2 System Description

2.1 General

The audio/modem hardware connects to the host processor via an AC-link interface. The OEM adds a 24.576 MHz crystal circuit if Primary AMC operation is required, optional digital speaker circuit, DIB components, LSD power rectifier and filter components, telephone line interface components, control straps, and other supporting discrete components as required and supported by the model to complete the system.

2.2 Hardware Description

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in world-wide markets by eliminating the need for country-specific components.

2.2.1 CX20468 Host Side Device

The CX20468 Host Side Device (HSD) serves as an AC'97 2.1 -compatible Audio Modem codec (AMC) packaged in a 48-pin TQFP. It can function as a primary or secondary AC-link codec as selected by the ID0#, ID1#, and PRIMARY_DN pins. As a primary codec, it uses an attached 24.576 MHz crystal to generate internal clocks and produce the 12.288 MHz AC-link bit clock (BIT_CLK). As a secondary codec, it uses an incoming 12.288 MHz BIT_CLK signal to generate its internal clocks.

Internal functions include an AC-link (AC'97) Interface, Power Management Interface, Caller ID Detection, Audio codec and a SmartDAA Interface.

AC-link Interface

The AC-link Interface connects directly to core logic or a PCI-based controller, typically through an CNR, ACR, AMR, MDC, or Mini PCI connector.

SmartDAA Interface

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

Audio Codec

Audio codec is compliant with AC'97 V2.1 specification.

2.2.2 Digital Isolation Barrier

The OEM-supplied Digital Isolation Barrier (DIB) electrically DC isolates the HSD from the LSD and telephone line. The HSD is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB power and clock transformer (PCXFMR) couples power and clock from the HSD to the LSD.

The DIB data channel supports bidirectional serial transfer of data, control, and status information between the HSD and the LSD.

2.2.3 CX20463 SmartDAA Line Side Device

The CX20463 SmartDAA Line Side Device (LSD) includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the HSD through the DIB.

LSD power is received from the DIB PCXFMR secondary winding through a half-wave rectifying diode and capacitive power filter circuit. The CLK input is also accepted from the PCXFMR secondary winding through a capacitor and a resistor in series. The LSD DGND is referenced to the bottom of the PCXFMR secondary winding.

Information is transferred between the LSD and the HSD through the DIB_P and DIB_N pins. These pins connect to the HSD DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-

hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and world-wide regulations and to actively control the DAA power dissipation.

2.3 Modem Operation

2.3.1 Host Modem Software

The host modem software performs the following tasks:

1. General modem control, which includes command sets, fax Class 1, voice/TAM, speakerphone through Conexant WDM driver, error correction, data compression, and operating system interface functions.
2. Modem data pump signal processing, which includes data and facsimile modulation and demodulation, as well as voice/TAM sample formatting.
3. SmartDAA control, which includes HSD SmartDAA Interface control, LSD configuration and control, telephone interface parameter control, and telephone line impedance control.

Configurations of the modem software are provided to support modem models listed in Table 1-1.

2.3.2 Data/Fax Modes

Modem operation, including dialing, call progress, telephone line interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

As a V.90/K56flex data modem, the modem can receive data from a digitally connected central site modem (CSM) at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data up to V.34 rates. This mode can fallback to full-duplex V.34 mode, and to lower rates as dictated by line conditions.

As a V.34 data modem, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the fax EIA/TIA-578 Class 1 and T.31 Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

2.3.3 Synchronous Access Mode (SAM) - Video Conferencing

V.80 synchronous access mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

2.3.4 Voice/TAM Mode

Voice/TAM Mode features include 8-bit μ-Law, A-Law, and linear coding at 8 kHz sample rates. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

Voice/TAM Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or, for speakerphone configuration, to a microphone/speaker.
2. Voice Receive Mode supports recording voice or audio data input from the telephone line or, for speakerphone configuration, from a microphone.
3. Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for speakerphone configuration, to a speaker.
4. Full-duplex voice supports concurrent voice receive and transmit.

2.4 Audio Operation

2.4.1 Host Audio Software

The Conexant Audio Software provides basic audio capability for all SmartAMC models (see Table 1-1). Optional enhanced audio and speakerphone features are also supported depending on SmartAMC model number and the host operating system.

- Basic Audio: Provides an AC'97 audio driver
- Enhanced audio – HRTF, EAX: Supports Head Related Transfer Function (HRTF) and Environmental Audio Extension (EAX)
- Enhanced audio - Conexant Player: Supports Soft Wavetable Support Conexant Player
- Speakerphone: Supports high quality, low latency soft speakerphone audio/modem HAL (Hardware Abstract Layer) based driver

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3 Hardware Interface

3.1 CX20468 HSD Hardware Pins and Signals

3.1.1 General

AC-link Host Interface

The AC-link host interface conforms to AC'97 rev 2.1 compatible for a single line Data/Fax/Voice/TAM only modem codec.

The supported AC-link signals are:

- Bit Clock (BIT_CLK), input/output
- Frame Sync (SYNC), input
- Serial Data Output (SDATA_OUT), input
- Serial Data Input 0 (SDATA_IN0), output
- Serial Data Input 1 (SDATA_IN1), output
- AC '97 Master Hardware Reset (AC_RESET#), input

Control Signals

Control signals supported from straps or the host are:

- Primary Down (PRIMARY_DN), input
- Codec ID (ID0# and ID1#); input

Audio Signals

Audio interface signals supported are:

- Microphone (MIC_IN), input
- CD Audio Left and Right Channel (CD_IN_L and CD_IN_R), input; and CD_IN_GND.
- Line In Left and Right Channel (LINE_IN_L and LINE_IN_R), input
- Line Out Left and Right Channel (LINE_OUT_L and LINE_OUT_R), output
- Headphone Out Left and Right Channel (HP_OUT_L and HP_OUT_R), output
- PC Speaker Beep Pass Through (PC_BEEP), input
- Sony Phillips Digital Interface (SPDIF_OUT), output

LSD Interface (Through DIB)

The supported DIB interface signals are:

- Clock and Power Plus (PWRCLKP); output
- Clock and Power Minus (PWRCLKN); output
- Data Plus (DIB_DATAP); input/output
- Data Minus (DIB_DATAN); input/output

Digital Speaker Interface

The digital speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode which can be optionally connected to an AC'97 audio device to enable playback of call progress through the analog mixer in the AC'97 device. The DSPKOUT output can be also be connected to a low-cost on-board speaker, e.g., a sounducer, without the use of an external op-amp.

3.1.2 Pin Assignments and Signal Definitions

The CX20468 HSD 48-pin TQFP hardware interface signals are shown by major interface in Figure 3-1, are shown by pin number in Figure 3-2, and are listed by pin number in Table 3-1.

The CX20468 HSD hardware interface signals are defined in Table 3-2.

The CX20468 HSD digital characteristics are defined in Table 3-3.

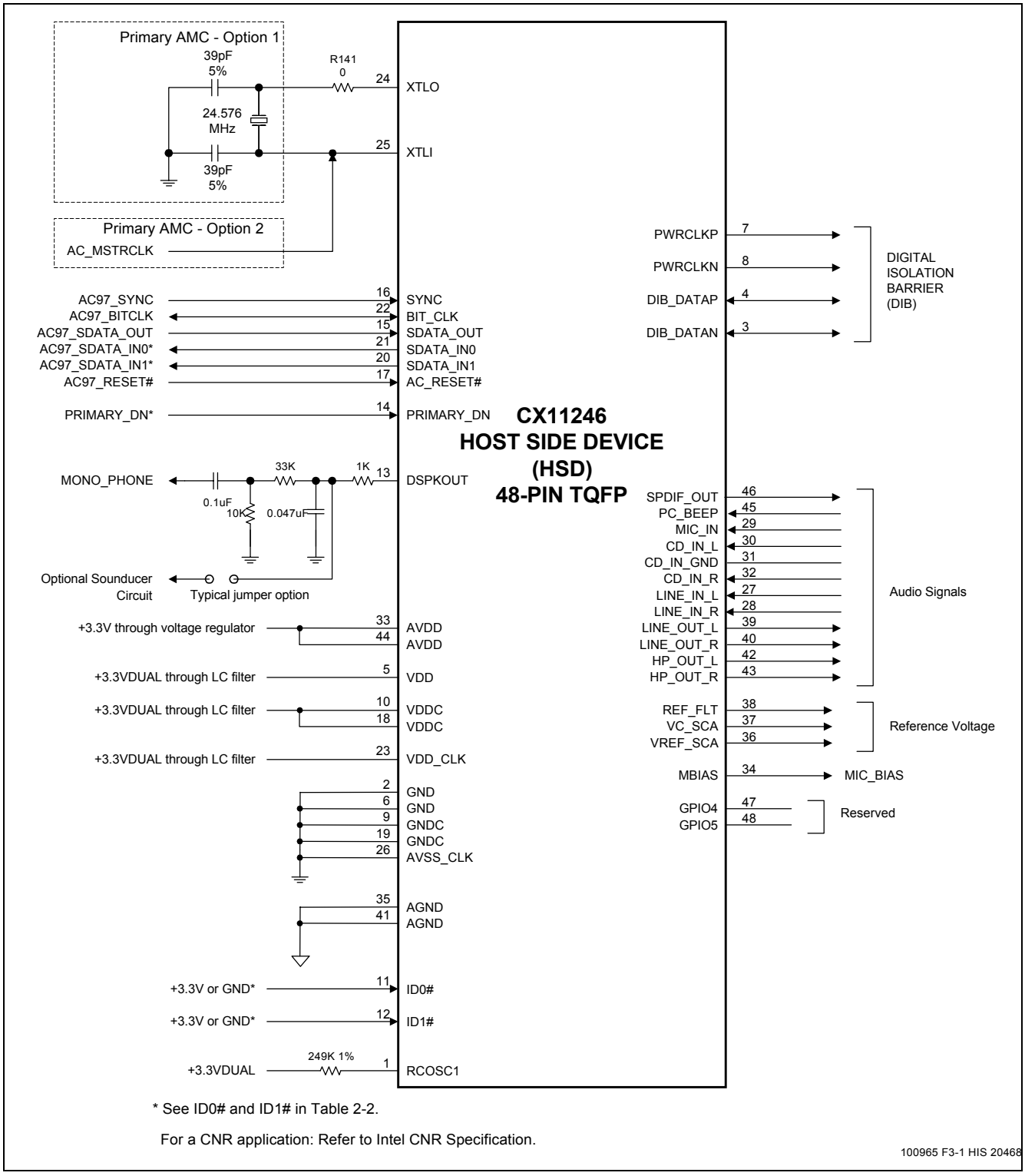


Figure 3-1. CX20468 HSD Hardware Interface Signals

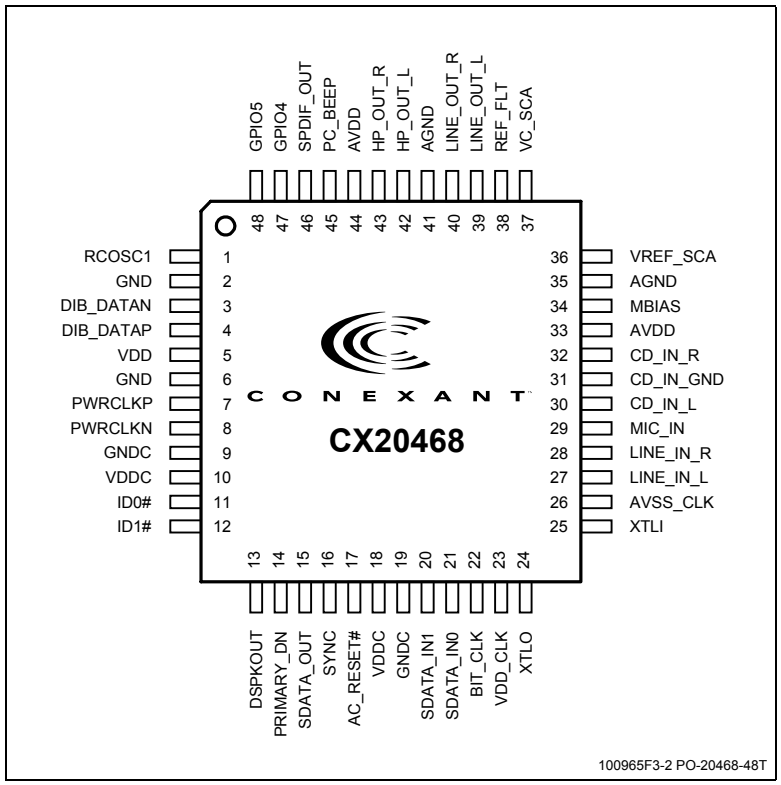


Figure 3-2. CX20468 HSD 48-Pin TQFP Pin Signals

Table 3-1. CX20468 HSD 48-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	RCOSC1		+3.3VDUAL through 249 KΩ, 1%	25	XTLI	Ix	For Primary AMC, 24.576 MHz crystal circuit or clock oscillator circuit (AC_MSTRCLK). For Secondary AMC, can be NC.
2	GND	GND	GND	26	AVSS_CLK	GND	GND
3	DIB_DATAN	Idd/Odd	DIB: Data Negative Channel capacitor	27	LINE_IN_L	Ia	AI: Line In Left Channel
4	DIB_DATAP	Idd/Odd	DIB: Data Positive Channel capacitor	28	LINE_IN_R	Ia	AI: Line In Right Channel
5	VDD	PWR	+3.3VDUAL through LC filter	29	MIC_IN	Ia	AI: Mic In
6	GND	GND	GND	30	CD_IN_L	Ia	AI: CD Audio Left Channel
7	PWRCLKP	Odpc	DIB: Primary Dotted Winding	31	CD_IN_GND	Ia	AI: CD Audio Ground
8	PWRCLKN	Odpc	DIB: Primary Undotted Winding	32	CD_IN_R	Ia	AI: CD Audio Right Channel
9	GNDC	GND	GND	33	AVDD	PWR	+3.3V through voltage regulator
10	VDDC	PWR	+3.3VDUAL through LC filter	34	MBIAS	O	MIC BIAS
11	ID0#	It	See ID0# and ID1# in Table 3-2	35	AGND	GND	AGND
12	ID1#	It	See ID0# and ID1# in Table 3-2	36	VREF_SCA	REF	AGND through 0.1 µF
13	DSPKOUT	Ot2	AI: Digital Speaker	37	VC_SCA	REF	AGND through 0.1 µF
14	PRIMARY_DN	It	See ID0# and ID1# in Table 3-2	38	REF_FLT	REF	AGND through 1 µF and 0.1 µF
15	SDATA_OUT	Iac	AC-link: AC97_SDATA_OUT	39	LINE_OUT_L	Oa	AI: Line Out Left Channel
16	SYNC	Iac	AC-link: AC97_SYNC	40	LINE_OUT_R	Oa	AI: Line Out Right Channel
17	AC_RESET#	Iac	AC-link: AC97_RESET	41	AGND	GND	AGND
18	VDDC	PWR	+3.3V DUAL through LC filter	42	HP_OUT_L	Oa	AI: Headphone Out Left Channel
19	GNDC	GND	GND	43	HP_OUT_R	Oa	AI: Headphone Out Right Channel
20	SDATA_IN1	Oac	See ID0# and ID1# in Table 3-2	44	AVDD	PWR	+3.3V
21	SDATA_IN0	Iac/Oac	See ID0# and ID1# in Table 3-2	45	PC_BEEP	Ia	AI: PC Speaker beep pass through
22	BIT_CLK	Iac/Oac	AC-link: AC97_BITCLK	46	SPDIF_OUT	Ot12	AI: SPDIF
23	VDD_CLK	PWR	+3.3VDUAL through LC filter	47	GPIO4	It/Ot12	NC
24	XTLO	Ox	For Primary AMC, 24.576 MHz crystal circuit, or leave open if XTLI is connected to clock circuit. For Secondary AMC, can be NC.	48	GPIO5	It/Ot12	NC

1. I/O types:

Iac	Digital input, AC-link-compatible, C_{IN} = 50 pF (see Table 3-3)
Iac/Oac	Digital input, AC-link-compatible, C_{IN} = 50 pF/Digital output, AC-link-compatible (see Table 3-3)
Idd/Odd	DIB data input/DIB data output
It	Digital input, TTL-compatible
Ix	Crystal input
Oac	Digital output, AC-link-compatible (see Table 3-3)
Odpc	DIB power and clock output
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ox	Crystal input

2. Interface Legend:

DIB	Digital Interface Barrier
AI	Audio interface
NC	No external connection

Table 3-2. CX20468 HSD Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
System			
VDD	5	PWR	**Digital Supply Voltage.** Connect to +3.3VDUAL through LC filter.
VDDC	10, 18	PWR	**Digital Supply Voltage.** Connect to +3.3VDUAL through LC filter
VDD_CLK	10, 18	PWR	**Digital Supply Voltage.** Connect to +3.3VDUAL through LC filter
AVDD	33, 44	PWR	**Analog Supply Voltage.** Connect to +3.3V through voltage regulator.
GND	2, 6	GND	**Digital Ground.** Connect to digital ground.
GNDC	9, 19	GND	**Digital Ground.** Connect to digital ground.
AVSS_CLK	26	GND	**Digital Ground.** Connect to digital ground.
AGND	35, 41	AGND	**Analog Ground.** Connect to analog ground.
XTLI	25	Ix	**Crystal In/Clock In.** For Primary AMC, connect to 24.576 MHz crystal circuit or clock oscillator circuit (AC_MSTRCLK). For Secondary AMC, pins can be left open.
XTLO	24	Ox	**Crystal Out.** For Primary AMC, connect to 24.576 MHz crystal circuit, or leave open if XTLI is connected to clock circuit. For Secondary AMC, pins can be left open.
ID0# ID1#	11 12	It It	**Codec ID.** Used in conjunction with PRIMARY_DN to select modem codec operation as a primary or secondary codec, as follows and shown in Figure 3-3: **For an ACR/AMR Riser Card:** 1. Connect PRIMARY_DN to GND. 2. Connect SDATA_IN0 to AC-link AC97_SDATA_IN0. 3. Connect SDATA_IN1 to AC-link AC97_SDATA_IN1. 4. Connect ID0# to AMR PRIMARY_DN#. 5. Leave ID1# open. If PRIMARY_DN# is low (codec is present on the motherboard), the ID is internally set to 01 for secondary codec operation and SDATA-IN1 is used. If PRIMARY_DN# is high (codec is not present on the motherboard), the ID is internally set to set to 00 for primary codec operation and SDATA-IN0 is used. **For a CNR application: Refer to Intel CNR Specification.** **For an MDC Board:** 1. Connect PRIMARY_DN to MDC PRIMARY_DN. 2. Connect SDATA_IN0 to SDATA_INA. 3. Connect SDATA_IN1 to motherboard SDATA_INB. 4. Leave ID0# open. 5. Leave ID1# open. The MDC SDATA_INA signal should be used whether or not there is a primary codec. PRIMARY_DN is high when audio codec is on the motherboard. **For a Mini PCI Board:** 1. Connect PRIMARY_DN to GND. 2. Connect SDATA_IN0 to SDATA_IN1. 3. Connect SDATA_IN0 to SDATA_IN1 to motherboard SDATA_IN. 4. Connect ID0# to Mini PCI Codec_ID0#. 5. Connect ID1# to Mini PCI Codec_ID1#.
RCOSC1	1		**RC Circuit 1.** Connect to +3.3VDUAL/+3.3VSB through 249 KΩ 1%.
MBIAS	34	O	**Microphone Bias.** This output provides a DC current for the microphone.
GPIO4 GPIO5	47 48	It/Ot12	**General Purpose I/O.** Reserved. If unused, connect to GND or +3.3V.

Table 3-2. CX20468 HSD Pin Signal Definitions (Continued)

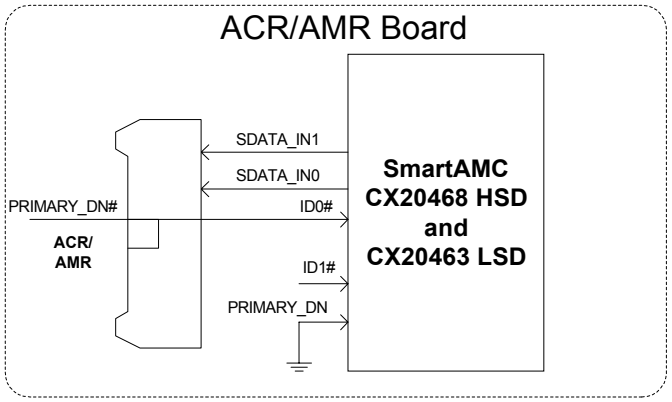
Signal Name	Pin	I/O Type	Description
Audio Analog Signals			
These signals connect the AC '97 component to analog sources and sinks, including microphones and speakers.			
SPDIF_OUT	46	Ot2	**Sony Phillips Digital Interface.** SPDIF mono output.
PC_BEEP	45	Ia	**PC Speaker Beep Pass through. When** RESET# is asserted, PC_BEEP is directly routed to the Line Out (LINE_OUT_L and LINE_OUT_R) through an internal 500 ohm resistor to allow the user to hear system startup beeps in the event of PC system errors. PC_BEEP is **not** routed to Line Level Output (HP_OUT_L and HP_OUT_R).
MIC_IN	29	Ia	**Microphone Input.** Connect to MIC.
CD_IN_L	30	Ia	**CD Audio Left Channel.** Connect through 10 µF AC-coupling capacitor.
CD_IN_GND	31	Ia	**CD Audio Analog Ground.** Connect through 10 µF AC-coupling capacitor.
CD_IN_R	32	Ia	**CD Audio Right Channel.** Connect through 10 µF AC-coupling capacitor.
LINE_IN_L	27	Ia	**Line In Left Channel.** Connect through 10 µF AC-coupling capacitor.
LINE_IN_R	28	Ia	**Line In Right Channel.** Connect through 10 µF AC-coupling capacitor.
LINE_OUT_L	39	Oa	**Line Out Left Channel.** Connect through 10 µF AC-coupling capacitor.
LINE_OUT_R	40	Oa	**Line Out Right Channel.** Connect through 10 µF AC-coupling capacitor.
HP_OUT_L	42	Oa	**Headphone Out/Line Level Out Left Channel.** Connect through 220 µF AC-coupling capacitor.
HP_OUT_R	43	Oa	**Headphone Out/Line Level Out Right Channel.** Connect through 220 µF AC-coupling capacitor.
Reference Voltage Connections			
REF_FLT	38	REF	**Reference Voltage Out.** Connect to AGND through 1 µF and 0.1 µF (ceramic) in parallel.
VREF_SCA	37	REF	**Reference Voltage.** Connect to AGND through 0.1 µF (ceramic).
VC_SCA	37	REF	**Reference Voltage.** Connect to AGND through 0.1 µF (ceramic).
DIB and SmartDAA Interface			
PWRCLKP	7	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD**.** Connect to the top of the DIB power and clock transformer primary winding.
PWRCLKN	8	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD**.** Connect to the bottom of the DIB power and clock transformer primary winding.
DIB_DATAP	4	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the HSD and LSD. Connect to the LSD through DIB data positive channel components.
DIB_DATAN	3	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the HSD and LSD. Connect to the LSD through DIB data negative channel components.

Table 3-2. CX20468 HSD Pin Signal Definitions (Continued)

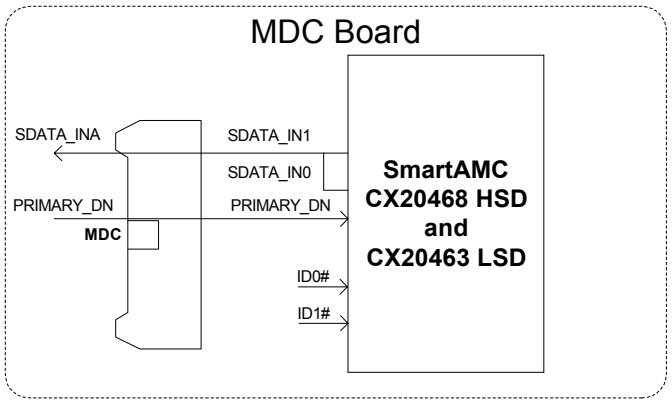
Label	Pin	I/O Type	Signal Name/Description
AC-link and AMR/MCD Interface			
BIT_CLK	22	Iac/Oac	**Bit Clock**. 12.288 MHz serial data output bit clock derived from a 24.576 MHz external crystal circuit when the AMC is configured as a primary codec. 12.288 MHz serial data input bit clock when the AMC is configured as a secondary codec. Connect to AC97_BITCLK through 33 Ω.
SYNC	16	Iac	**Frame Sync.** 48 kHz fixed rate sample AC-link sync input. Synchronization pulse from an AC'97 compliant controller to all of the AC'97 compliant codecs on the link. This signal is nominally 1.3 μs wide pulse that is used to synchronize the AC-link. Reset state = low. Standard load = 50 pF. Connect to AC97_SYNC.
SDATA_OUT	15	Iac	**Serial Data Output.** Serial, time division multiplexed, input data stream from an AC'97 controller. Reset state = low. Standard load = 50 pF. Connect to AC97_SDATA_OUT through 33 Ω.
SDATA_IN0	21	Oac	**Serial Data Input 0.** Serial, time division multiplexed, output data stream. Output data stream to an AC'97 controller when the SmartAMC is a Primary AMC. See ID0# and ID1# description in this table and Figure 3-3. Connect to AC97_SDATA_ IN0 through 33 Ω.
SDATA_IN1	20	Oac	**Serial Data Input 1.** Serial, time division multiplexed, output data stream to an AC'97 controller when the SmartAMC is a Secondary AMC. See ID0# and ID1# description in this table and Figure 3-3. Connect to AC97_SDATA IN1 through 33 Ω.
AC_RESET#	17	Iacl	**AC '97 Master Hardware Reset.** Active low reset. Reset state = low. Standard load = 50 pF. Connect to AC97_RESET.
PRIMARY_DN	14	It	**Primary Down**. Used in conjunction with ID0# and ID1# to select modem codec operation as a primary or secondary codec. See ID0# and ID1# description in this table and Figure 3-3.
DSPKOUT	13	Ot12	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator. Connect to the MONO_PHONE signal through a filter circuit and optionally to an on-board speaker circuit, e.g., sounducer. The DSPKOUT output is used for call progress monitoring.

Notes:

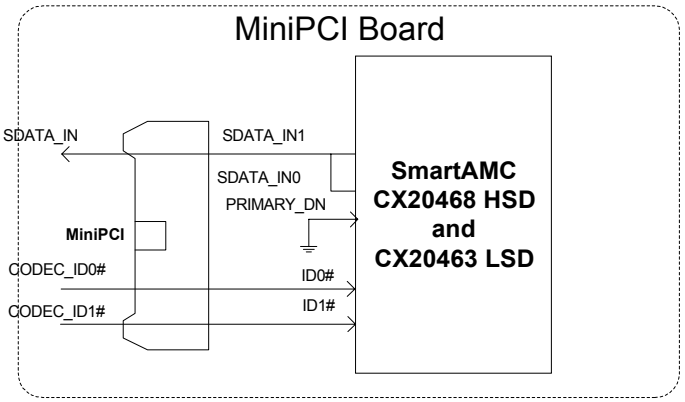
1. I/O types:
   - Iac — Digital input, AC-link-compatible, C_{IN} = 50 pF (see Table 3-3)
   - Iac/Oac — Digital input, AC-link-compatible, C_{IN} = 50 pF/Digital output, AC-link-compatible (see Table 3-3)
   - Idd/Odd — DIB data input/DIB data output
   - It — Digital input, TTL-compatible
   - Ix — Crystal input
   - Oac — Digital output, AC-link-compatible (see Table 3-3)
   - Odpc — DIB power and clock output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - Ox — Crystal input
2. Interface Legend:
   - DIB — Digital Interface Barrier
   - NC — No external connection



a. SmartAMC ACR/AMR Connection



b. SmartAMC MDC Connection



c. SmartAMC Mini PCI Connection

100965 F3-3 Conn

Figure 3-3. Modem Codec Primary/Secondary Codec Connections

Table 3-3. CX20468 HSD Digital Electrical Characteristics - AC-link

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage	V_{IN}	-0.30	–	3.60	VDC	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	VDC	
Input Voltage High	V_{IH}	1.6	–	–	VDC	
Output Voltage Low	V_{OL}	0	–	0.33	VDC	
Output Voltage High	V_{OH}	2.97	–	–	VDC	
Input Leakage Current (AC-link inputs)	–	-10	–	10	µA	
Output Leakage Current (High-Z AC-link outputs)	–	-10	–	10	µA	

Notes:
1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.

Table 3-4. CX20468 HSD Digital Electrical Characteristics –TTL - Compatible

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IL}	-0.3	–	0.8	VDC	
Input Voltage High	V_{IH}	2.0	–	3.6	VDC	
Input Current Low (See Note 2)	I_{IL}	–	–	-10	µA	V_{IN} = 0
Input Current High (See Note 2)	I_{IH}	–	–	+10	µA	V_{IN} = +3.6V

Notes:
1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C.
2. Current flow out of the device is shown as minus.

Table 3-5. CX20468 HSD DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Voltage	V_{in}	-0.30	-	3.60	V	VDD = +3.6V
Input Voltage Low	V_{il}	-0.30	-	0.25*VDD	V	
Input Voltage High	V_{ih}	0.65*VDD	-	VDD + 0.3	V	
Output Voltage Low	V_{ol}	0	-	0.1*VDD	V	
Output Voltage High	V_{oh}	0.85*VDD	-	VDD	V	
GPIO Output sink current at 0.4 V maximum	-	2.4	-	-	mA	
GPIO Output source current at 2.97 V minimum	-	2.4	-	-	mA	
GPIO rise/fall time		20		100	ns	

Notes:
1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; T_A = 0°C to 70°C; external load = 50 pF

Table 3-6. CX20468 HSD Analog Performance Characteristics

Parameter	Min	Typical	Max	Units
Full Scale Input Voltage				
LINE_IN	-	1.0	-	Vrms
MIC (+20 dB Boost on)	-	0.1	-	Vrms
MIC (+20 dB Boost off)	-	1.0	-	Vrms
Full Scale Output Voltage				
LINE_OUT	-	1.0	-	Vrms
HP_OUT	-	1.0	-	Vrms
Analog S/N				
CD to LINE_OUT, HP_OUT, or MONO_OUT	90	-	-	dB
Other to LINE_OUT, HP_OUT, or MONO_OUT	-	85	-	dB
Analog Frequency Response (±1 dB limits)	20	-	20,000	Hz
Digital S/N[1]				
D/A	85	90	-	dB
A/D	75	80	-	dB
Total Harmonic Distortion:				
LINE_OUT (0 dB gain, 20 kHz BW, 48 kHz Sample Frequency)	-	-	0.02	%
HP_OUT (+0 dB output into 32 Ω load)	-	-	0.5	%
D/A and A/D Frequency Response (±0.25 dB limits)	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[2]	-74	-	-	dB
Out-of-Band Rejection[3]	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk between Input channels	-	-	-70	dB
Crosstalk between headphone channels	-	-	-70	dB
Crosstalk between line ADC/DAC and any other channel	-	-	-80	dB
Isolation between audio and modem sections	80	-	-	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size (except for PC Beep)	-	1.5	-	dB
Interchannel Gain Mismatch (Difference between errors)	-0.5	-	0.5	dB
Absolute Gain Step Error at any given setting	-	-	0.75	dB
Input Resistance	10	-	-	Kohm
Input Capacitance	-	7.5	-	pF
Vrefout	-	2.5-2.8	-	V
DC Offset				
Audio ADCs	-	±10	±50	mV
Other ADCs	-	-	±100	mV
Audio DACs	-	±5	±25	mV
Other DACs	-	-	±100	mV

Table 3-6. CX20468 HSD Analog Performance Characteristics (Continued)

Parameter	Min	Preliminary	Max	Units
Modem Line				
DAC to Line Driver output SNR at -10 dBm, 1200 Ω	77	-	80	dB
Line Input to ADC SNR at -6 dBm	77	-	80	dB
Mic ADC				
Line Input to ADC SNR at -6 dBm without 20 dB boost	77	-	80	dB
Line Input to ADC SNR at -6 dBm with 20 dB boost	-	65	-	dB

Notes

1. The ratio of the rms output level with 1kHz full scale input to the rms output level with all zeros into the digital input. Measured “A wtd” over a 20Hz to a 20kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
2. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
3. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 VRMS DAC output.

Standard test conditions unless otherwise noted:

- Temperature 25 °C
- Analog Supply (AVDD) 3.3 V ±0.3V
- Digital Supply(VDD) 3.3 V ±0.3V
- Input Voltage Levels: VDD = +3.3 V
  - Logic Low 0.8 V
  - Logic High 2.4 V
- Input signal 1 kHz sine wave
- Sample Frequency(FS) 48 kHz
- 0 dBV = 1 Vrms
- 10 kohm/50 pF load
- Testbench Characterization BW:
  - Pass Band 20 Hz - 20 kHz
  - Attenuation 0 dB
  - Gain on inputs 0 dB

3.1.3 AC Timing Characteristics

AC Link Clocks

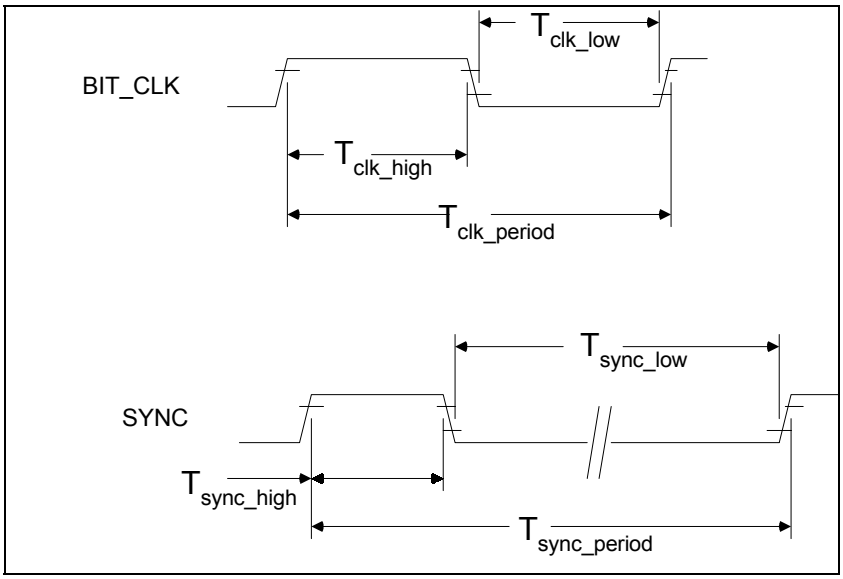


Figure 3-4. BIT_CLK and SYNC Timing Waveforms

Table 3-7. BIT_CLK and SYNC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (Note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs

Notes
1. Worst case duty cycle restricted to 45/55.
2. 47.5-70 pF external load.

Data Output and Input

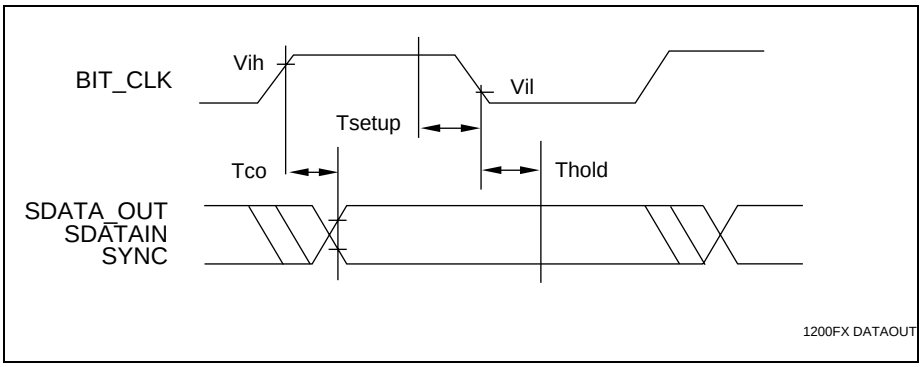


Figure 3-5. Data Output and Input Timing Waveforms

Table 3-8. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	Tco	-	-	15	ns
Notes 1. Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. 2. 50 pF external load.					

Table 3-9. AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	T_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	T_{hold}	10	-	-	ns
Note Timing is for SDATA and SYNC inputs with respect to BIT_CLK at the device latching the input.					

Table 3-10. AC-link BIT_CLK and SDATA Rise and Fall Time Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note Maximum combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					

Signal Rise and Fall Times

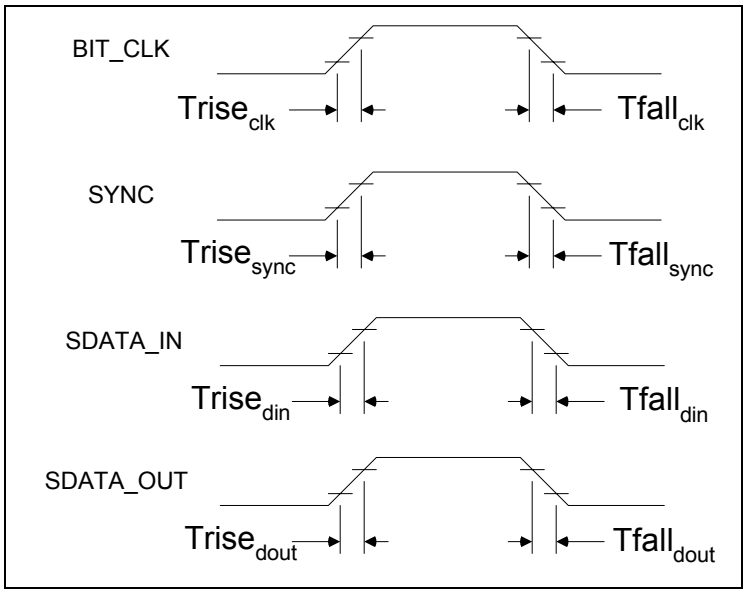


Figure 3-6. Signal Rise and Fall Time Timing Waveforms

Table 3-11. Signal Rise and Fall Time Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns

Notes
1. 50pF external load; from 10% to 90% of VDD.
2. rise is from 10% to 90% of VDD (Vol to Voh).
3. fall is from 90% to 10% of VDD (Voh to Vol).

RESET# (Cold Reset)

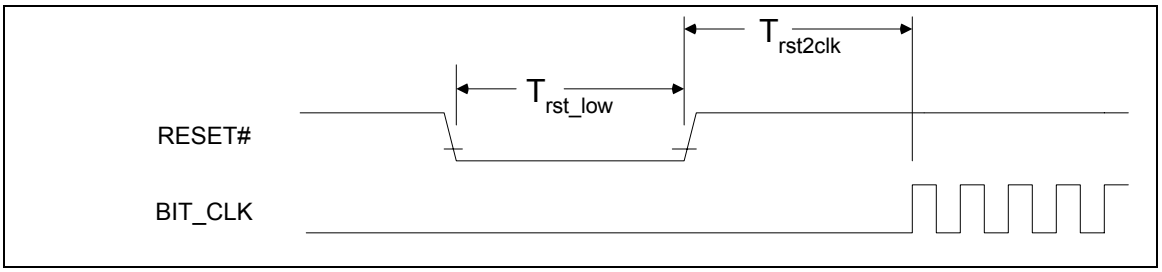


Figure 3-7. Cold Reset Timing Waveforms

Table 3-12. Cold Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

RESET# (Warm Reset)

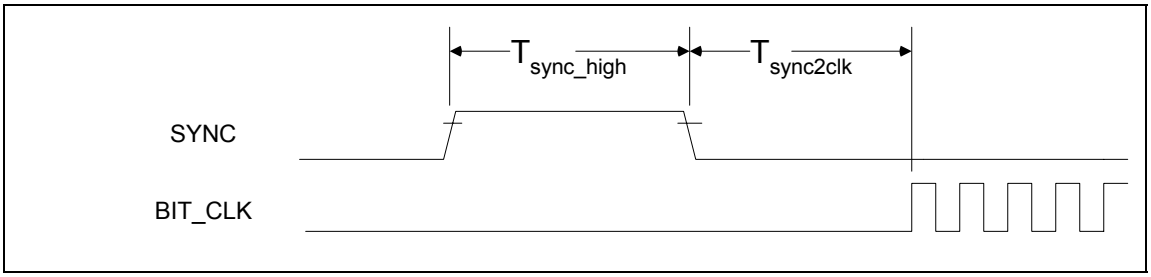


Figure 3-8. Warm Reset Timing Waveforms

Table 3-13. Warm Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

Note
The minimum SYNC pulse width pertains to warm reset only, during normal operation, SYNC is asserted for the entire tag phase (16 BIT_CLK times).

AC-link Low Power Mode Timing

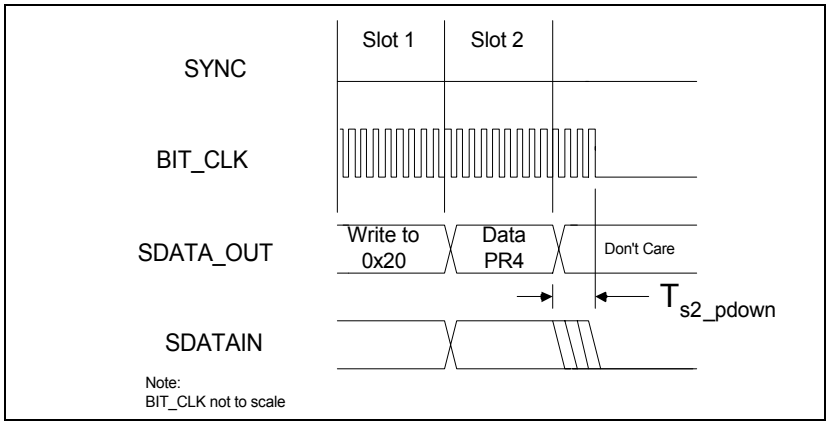


Figure 3-9. AC-link Low Power Mode Timing Waveforms

Table 3-14. AC-link Low Power Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

ATE Test Mode Timing

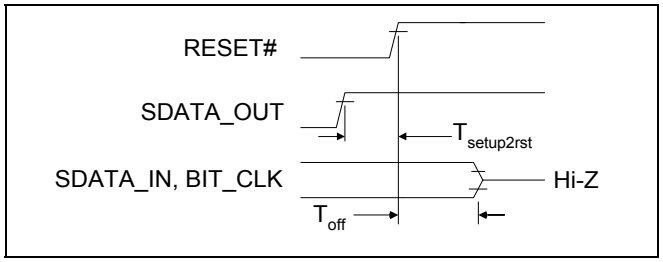


Figure 3-10. ATE Test Mode Timing Waveforms

Table 3-15. ATE Test Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

3.1.4 AC-link IO Pin Capacitance and Loading

In multiple Codec implementations, the AC '97 2.1 Controller can drive SYNC and SDATA_OUT to two or more destinations. The Controller's SYNC and SDATA_OUT output pin drivers must meet AC-link timing requirements when loaded by the total capacitance on each of these outputs.

In multiple Codec implementations, the SmartAMC can drive BIT_CLK to 1 or 2 destinations. The Codec's BIT_CLK output pin driver meets AC-link timing requirements when loaded by the total capacitance on this output.

- The following factors contribute to total capacitance:
- Controller or Codec output pin capacitance (internal device characteristic)
- Codec or Controller input pin capacitance (7.5 pF max per AC '97 2.1, see Table 3-16)
- Total trace length capacitance on motherboard plus riser (estimated 2.5 pF per inch). Note that motherboard plus riser trace lengths, especially in multiple Codec implementations such as AC down (motherboard) and MC up (riser), could exceed ~15 inches.
- IO connectors, such as motherboard to riser (estimated 2.5 pF)

AC '97 2.1 compatibility recommends that the following Controller and Codec input pins have a maximum of 7.5 pF capacitance:

- Controller BIT_CLK and SDATA_IN[0-3] inputs
- Primary and Secondary Codec SYNC and SDATA_OUT inputs
- Secondary Codec BIT_CLK input

AC '97 2.1 compatibility recommends the Controller and Codec AC-link output pin drivers identified in Table 3-16 be of sufficient strength to meet AC-link timing requirements for the following specified external capacitive loads in 1-4 Codec implementations. In addition to these external capacitive loads, additional allowance must be made for the particular Controller or Codec output pin capacitance (internal device characteristic).

Table 3-16. AC-link Pin IO Driver Loading

Output pin	Capacitance: 1 Codec	Capacitance: 2 Codecs
Controller: SYNC, SDATA_OUT	47.5 pF	55 pF
Codec: BIT_CLK (can support 2 codecs)	55 pF	55 pF
Codec: SDATA_IN (point to point)	47.5 pF	47.5 pF
Notes: 47.5 pF load comprehends 1 input, 1 connector, and ~15 inches of trace length. 55 pF load comprehends 2 inputs, 1 connector, and ~15 inches of trace length.		

3.1.5 Crystal Specification

Table 3-17 lists the required crystal parameters.

Table 3-17. Crystal Specification

Parameter	Range
Frequency	24.576 MHz
Oscillation Mode	Fundamental
Resonance	Parallel
Load Capacitance	22 pF
Frequency Tolerance	± 40 ppm @ 25 °C
Temperature Stability	± 45 ppm, 0-70 °C
Operating Temperature	0 -70 °C
Shunt Capacitance	< 7 pF
Equivalent Series Resistance	< 35 ohms @ 20 nW Drive Level
Drive Level	100 µW Correlation, 300 µW Max
Aging	± 15 ppm over 5 years
Storage Temperature Range	-40 to +85 °C

3.2 CX20463 LSD Hardware Pins and Signals

3.2.1 General

HSD Interface (Through DIB)

The DIB interface signals are:

- Clock (CLK); input
- Digital Power (PWR+); input power
- Digital Ground (DGND); digital ground
- Data Positive (DIB_P); input
- Data Negative (DIB_N); input

Telephone Line Interface

The telephone line interface signals are:

- RING AC Coupled (RAC1); input
- TIP AC Coupled (TAC1); input
- RING AC Coupled (RAC2); input
- TIP AC Coupled (TAC2); input
- Electronic Inductor Resistor (EIR); output
- TIP and RING DC Measurement (TRDC); input
- DAC Output Voltage (DAC); output
- Electronic Inductor Capacitor (EIC)
- Electronic Inductor Output (EIO)
- Electronic Inductor Feedback (EIF)
- Resistive Divider Midpoint (DCF)
- Transmit Analog Output (TXA); output
- Receive Analog Input (RXI); input
- Receiver Gain (RXG); output
- MOV Enable (MOVEN); output
- World-wide Impedance 0 (ZW0); input
- US Impedance 0 (ZUS0); input
- Transmit Feedback (TXF); input
- Transmit Output (TXO); output

3.2.2 Pin Assignments and Signal Definitions

The CX20463 LSD 32-pin TQFP hardware interface signals are shown by major interface in Figure 3-11, are shown by pin number in Figure 3-12, and are listed by pin number in Table 3-18.

The CX20463 LSD hardware interface signals are defined in Table 3-19.

The CX20463 LSD digital characteristics are specified in Table 3-20.

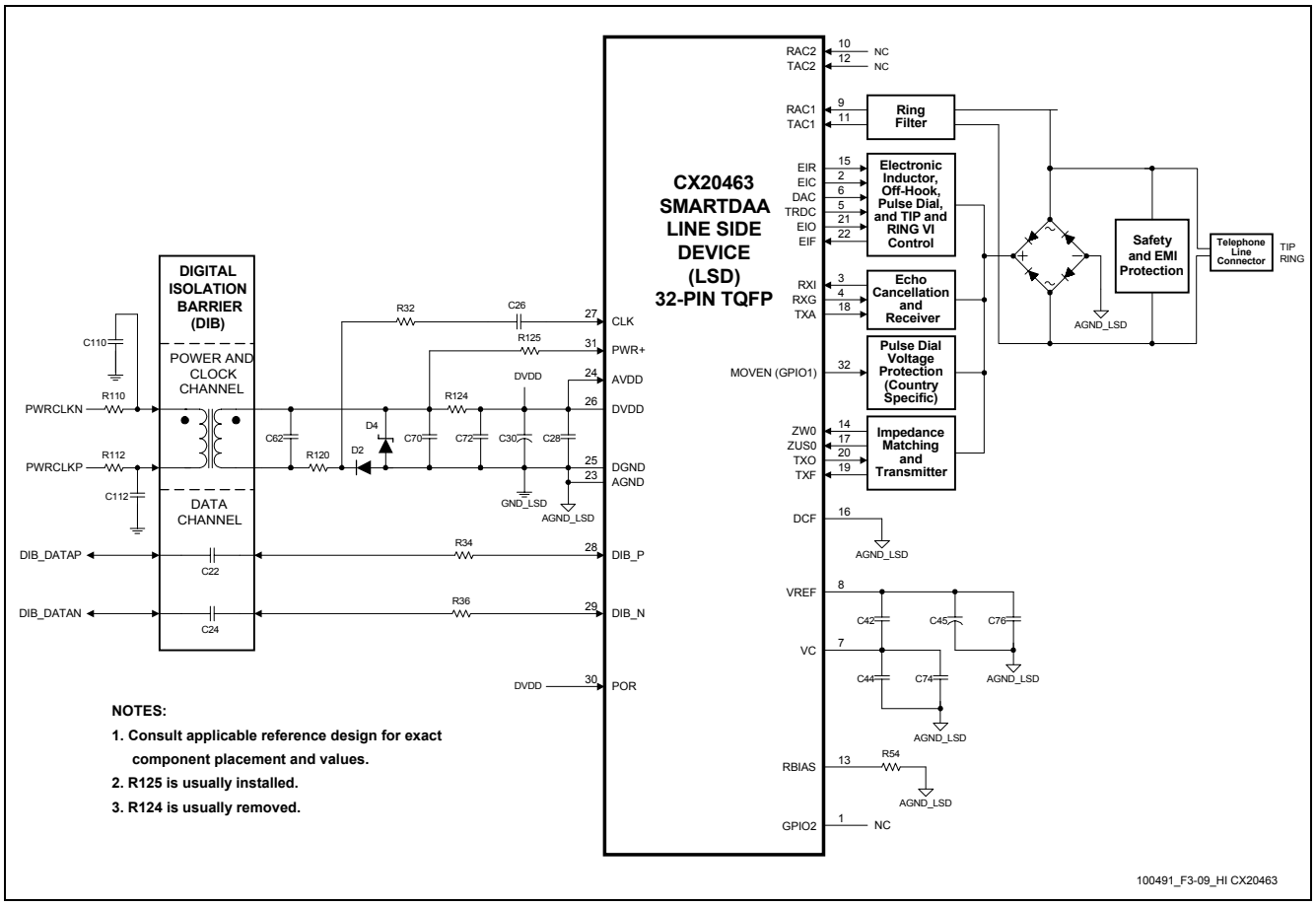


Figure 3-11. CX20463 LSD Hardware Interface Signals

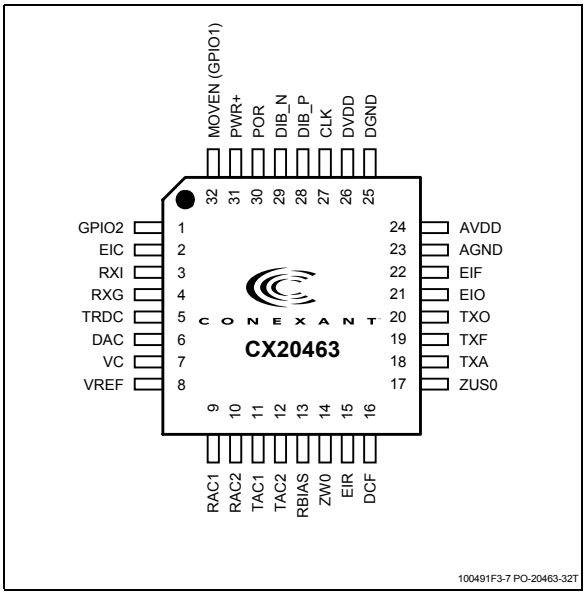


Figure 3-12. CX20463 LSD 32-Pin TQFP Pin Signals

Table 3-18. CX20463 LSD 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface
1	GPIO2	It/Ot12	NC
2	EIC	Oa	Telephone Line Interface Components
3	RXI	Ia	Telephone Line Interface Components
4	RXG	Oa	Telephone Line Interface Components
5	TRDC	Oa	Telephone Line Interface Components
6	DAC	Oa	Telephone Line Interface Components
7	VC	REF	VREF through C42 and to AGND_LSD through C44 and C76
8	VREF	REF	VC through C42 and to AGND_LSD through C45 and C76
9	RAC1	Ia	Diode bridge top through R2 and C2
10	RAC2	Ia	NC
11	TAC1	Ia	Diode bridge bottom through R4 and C4
12	TAC2	Ia	NC
13	RBIAS	Ia	AGND_LSD through R54
14	ZW0	Ia	Telephone Line Interface Components
15	EIR	Ot12	Telephone Line Interface Components
16	DCF	Ia	AGND_LSD
17	ZUS0	Ia	Telephone Line Interface Components
18	TXA	Oa	Telephone Line Interface Components
19	TXF	Ia	Telephone Line Interface Components
20	TXO	Oa	Telephone Line Interface Components
21	EIO	Oa	Telephone Line Interface Components
22	EIF	Ia	Telephone Line Interface Components
23	AGND	AGND_LSD	AGND_LSD
24	AVDD	PWR	LSD DVDD pin
25	DGND	GND_LSD	DIB transformer secondary winding undotted terminal through diode D2 and R120 in series and to GND_LSD
26	DVDD	PWR	LSD AVDD pin, to GND_LSD through C28, C30, and C72 in parallel.
27	CLK	I	DIB transformer secondary winding undotted terminal through C26 and R32 in series and through R120 shared with LSD DGND pin through diode D2
28	DIB_P	I/O	DIB C22 through R34
29	DIB_N	I/O	DIB C24 through R36
30	POR	It	LSD DVDD pin
31	PWR+	PWR	DIB transformer secondary winding dotted terminal through R125 and to GND_LSD through zener diode D4 and C70 in parallel
32	MOVEN (GPIO1)	Ot12	Telephone Line Interface Components

Notes:

1. I/O types*:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground

   *See CX20463 LSD Digital Electrical Characteristics (Table 3-20).
2. Interface Legend:
   - HSD — Host Side Device
3. Refer to applicable reference design for exact component placement and values.

Table 3-19. CX20463 LSD Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
AVDD	24	PWR	**Analog Power Supply.** Connect to the LSD DVDD pin.
AGND	23	AGND_LSD	**LSD Analog Ground. LSD Analog Ground.** Connect to AGND_LSD at the GND_LSD/AGND_LSD tie point and to the analog ground plane.
POR	30	It	**Power-On Reset.** Connect to LSD DVDD pin.
VREF	8	REF	**Output Reference Voltage.** Connect to VC through C42 and to AGND_LSD through C45 and C76. Ensure a very close proximity between C42 and C45 and the VREF pin.
VC	7	REF	**Output Middle Reference Voltage.** Connect to VREF through V42 and to AGND_LSD through C44 and C74. Ensure a very close proximity between C44 and the VC pin. Use a short path and a wide trace to AGND_LSD pin.
DIB INTERFACE SIGNALS			
CLK	27	I	**Clock.** Provides input clock, AC-coupled, to the LSD**.** Connect to DIB transformer secondary winding undotted terminal through R32 and C26 in series and through R120 shared with LSD DGND pin through diode.
PWR+	31	PWR	**Digital Power Input**. Provides unregulated input digital power to the LSD. Connect to DIB transformer secondary winding dotted terminal through R125, and to GND_LSD though zener diode D4 and C70 in parallel.
DVDD	26	PWR	**Digital Power**. Connect to pin 24 (AVDD), to DIB transformer secondary winding dotted terminal through R124, and to GND_LSD through C28, C30, and C72 in parallel.
DGND	25	GND_LSD	**LSD Digital Ground.** Connect to DIB transformer secondary winding undotted terminal through diode D2 in series with R120, and to GND_LSD at the GND_LSD/AGND_LSD tie point.
DIB_P	28	I/O	**Data and Control Positive.** Connect to HSD DIB_DATAP through C22 in the DIB and R34 on the LSD side. DIB_P and DIB_N signals are differential, and ping-pong between DIB and HSD (half duplex).
DIB_N	29	I/O	**Data and Control Negative.** Connect to HSD DIB_DATAN through C24 in the DIB and R36 on LSD side and 100 pF in DIB. DIB_P and DIB_N signals are differential, and ping-pong between DIB and HSD (half duplex).
TIP AND RING INTERFACE			
RAC1, TAC1	9, 11	Ia, Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC-coupled voltage from telephone line used to detect ring. Connect RAC1 to the top of the diode bridge through R2 and C2 Connect TAC1 to the bottom of the diode bridge through R4 and C4.
RAC2 TAC2	10, 12	Ia, Ia	**RING2 AC Coupled and TIP2 AC Coupled.** Not used; leave open.
EIR	15	Oa	**Electronic Inductor Resistor.** Electronic inductor resistor switch.
EIC	2	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to no connect when pulse dialing and to ground all other times. This is needed to eliminate pulse dial interference from the electronic inductor AC filter capacitor.
DAC	6	Oa	**DAC Output Voltage.** Output voltage of the reference DAC.
TRDC	5	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information.
EIO	21	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control offhook, pulse dial, and DC IV mask operation.
EIF	22	Ia	**Electronic Inductor Feedback.** Electronic inductor feedback.
RXG	4	Oa	**Receiver Gain.** Receiver gain output.
RXI	3	Ia	**Receive Analog Input.** Receive signal input.
TXA	18	Oa	**Transmit Analog Output.** Transmit signal used for canceling echo in the receive path.
MOVEN (GPIO1)	32	Ot12	**MOV Enable**. Connect to pulse dial voltage protection circuit for Australia/Poland/Italy use. Leave open if the product is not intended for Australia, Poland, or Italy.
RBIAS	13	Ia	**Receiver Bias.** Connect to GND through R54.
DCF	16	Ia	**Resistive Divider Midpoint.** Connect to LSD analog ground.

Table 3-19. CX20463 LSD Pin Signal Definitions (Continued)

Label	Pin	I/O Type	Signal Name/Description
TELEPHONE LINE INTERFACE (CONTINUED)			
ZW0	14	Ia	**World-Wide Impedance 0.** Input signal used to provide line complex impedance matching for world-wide countries.
ZUS0	17	Ia	**US Impedance 0.** Input signal used to provide line impedance matching for U.S.
TXO	20	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to transmitter transistor.
TXF	19	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor.
NOT USED			
GPIO2	1	It/Ot12	**General Purpose I/O 2**. Leave open if not used.

Notes:

1. I/O types*:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground

   *See CX20463 LSD Digital Electrical Characteristics (Table 3-20).
2. Interface Legend:
   - HSD — Host Side Device
3. Refer to applicable reference design for exact component placement and values.

Table 3-20. CX20463 LSD Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	3.60	V	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.4 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF

3.3 Electrical and Environmental Specifications

The operating conditions are specified in Table 3-21.

The absolute maximum ratings are listed in Table 3-22.

The current and power requirements are listed in Table 3-23.

Table 3-21. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	+3.0 to +3.6	VDC
Operating Temperature Range	T_A	0 to +70	°C

Table 3-22. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.0	V
Input Voltage	V_{IN}	-0.5 to (VIO +0.5)*	V
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA + 0.5)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VIO +0.5)*	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VIO = +3.3V ± 0.3V or +5V ± 5%.			

Table 3-23. Current and Power Requirements

Device State (Dx)	Conditions			Current		Power	
	AC-link	HSD Crystal**	DIB Clocks*	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)
CX20468 HSD + CX20463 LSD							
D0—Port Closed	On	On	On	TBD	TBD	TBD	TBD
D0—Port Open	On	On	On	TBD	TBD	TBD	TBD
D0—On-Line	On	On	On	TBD	TBD	TBD	TBD
D3—Suspend	Off	Off	On	TBD	TBD	TBD	TBD
D3—Suspend	Off	Off	Off*	TBD	TBD	TBD	TBD

Notes:

Operating voltage: VDD = +3.3V Dual/Standby.

Definitions:

Device State: D0 = Full power state; D3 = Low power state.

AC-link: The AC-link is considered off upon removal of the BIT_CLK.

*DIB Clocks: On = The DIB clocks must be on (i.e., digital interface between the system-side and line-side is operating) to wake from ring or to capture Caller ID.

** HSD Crystal control applies to Primary operation only. For Secondary operation, the AC-link provides the device clock.

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4 AMC Interface Registers

Table 4-1 identifies the AMC registers and bits.

Table 4-1. Audio Modem Codec (AMC) Registers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	x	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0152h
02h	Play Master Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0000h
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	x	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	x	x	x	x	x	x	x	x	LPBK	x	x	x	x	x	x	x	0000h
26h	Powerdown Control/Status	x	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	x	PDA	x	**REF**	**ANL**	**DAC**	**ADC**	400xh
28h	Extended Audio ID	**ID1**	**ID0**	x	x	x	x	**AMAP**	**LADC**	**SDAC**	**CDAC**	x	x	**VRM**	x	**DRA**	**VRA**	x201h
2Ah	Extended Audio Status/Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	VRA	0000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ch	Extended Modem ID	**ID1**	**ID0**	x	x	x	x	x	x	x	x	x	**CID2**	**CID1**	**HSET**	**LIN2**	**LIN1**	x001h
3Eh	Extended Modem Status/Control	x	x	x	x	x	x	x	PRA	x	x	x	x	x	x	x	**GPIO**	010xh
40h	Modem Line 1 ADC/DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
4Ch	GPIO Pin Configuration	x	x	x	x	x	x	x	x	x	x	GC5	GC4	x	x	x	x	0030h
4Eh	GPIO Pin Polarity/Type	x	x	x	x	x	x	x	x	x	x	GP5	GP4	x	x	x	x	FFFFh
50h	GPIO Pin Sticky	x	x	x	x	x	x	x	x	x	x	GS5	GS4	x	x	x	x	0000h
52h	GPIO Pin Wake up	x	x	x	x	x	x	x	x	x	x	GW5	GW4	x	x	x	x	0000h
54h	GPIO Pin Status	x	x	x	x	x	x	x	x	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	00xxh
56h	Misc Modem AFE Status/Control	x	x	x	MLNK	x	x	x	x	x	x	x	x	x	x	x	x	0000h
5Ah	Mixer Volume	x	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h
5Ch	Miscellaneous Audio	x	x	x	x	x	MuteLvl	PdLvl	PdMicB	x	MicSel	DacSel1	DacSel0	SPDifEn	CpRight	Mode1	Mode0	0600h
66h	DIB Control	x	**DRDB1**	x	INTE1	x	**RG1**	x	**RGIE1**	x	x	PDDXE	CTBSY	IRAR	x	PDX	x	x00xh
68h	Cold Reset Mask	CMR15	CMR14	CMR13	CMR12	CMR11	CMR10	CMR9	CMR8	CMR7	CMR6	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	xxxxh
6Ah	CID Time Out	x	x	x	x	x	x	x	x	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	0040h
72h-76h	Conexant Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	xxxxh
7Ah	Indexed1 Register	IRWB	IADDR6	IADDR5	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	**IDAT7**	**IDAT6**	**IDAT5**	**IDAT4**	**IDAT3**	**IDAT2**	**IDAT1**	**IDAT0**	80xxh
7Ch	Vendor ID1	**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	4358h
7Eh	Vendor ID2	**T7**	**T6**	**T5**	**T4**	**T3**	**T2**	**T1**	**T0**	**REV7**	**REV6**	**REV5**	**REV4**	**REV3**	**REV2**	**REV1**	**REV0**	5428h

Bold: Read-only inputs to AC-link.

4.1 Register Definitions

4.1.1 Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers belonging to audio subsystem (00h-38h, 5Ah, and 5Ch) to revert to their default values. Reading this register returns the ID code identifying supported functions and a code identifying the supported 3D Stereo Enhancement Technique.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	x	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0152h

Bit	Label	R/W	Description
15			**Reserved.** Set to 0.
14:10	SE[4:0]	R	**3D Stereo Enhancement.** 00000b = Not supported.
9	ID9	R	**20-Bit ADC Supported Status.** 0 = Not supported.
8	ID8	R	**18-Bit ADC Supported Status.** 1 = Supported.
7	ID7	R	**20-Bit DAC Supported Status.** 0 = Not supported.
6	ID6	R	**18-Bit DAC Supported Status.** 1 = Supported. All stereo DACs and ADCs operate at 18-bits of resolution.
5	ID5	R	**Loudness (Bass Boost) Supported Status** 0 = Not supported.
4	ID4	R	**Headphone Out Supported Status.** 1 = Supported (LNLVL_OUT is supported).
3	ID3	R	**Simulated Stereo (Mono to Stereo) Supported Status.** 0 = Not supported.
2	ID2	R	**Bass and Treble Control Supported Status.** 0 = Not supported.
1	ID1	R	**Modem Line Codec Supported Status.** 1 = Supported (this bit must be set when a register reset occurs).
0	ID0	R	**Dedicated Mic PCM in Channel Supported Status.** 0 = Not supported. However, received data from analog Microphone input can be selectively routed to AC-link slot 6 by setting MicSel control bit (bit 6 of register 5Ch).

4.1.2 Play Master Volume Register (Index 02h)

This register controls the Play Master output volume. The AC'97 spec describes bit 5 being optional, meaning attenuation values of 48 to 94.5 dB is optional. This bit is not supported. However, 1.5dB step sizes are required.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Play Master Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Master Volume Mute.** 0 = Channel volume is controlled by the ML[4:0] and MR[4:0] bits). 1 = The channel is muted. (Default.)
14:13			**Reserved.**
12:8	ML[4:0]	R/W	**Left Master Volume Control Attenuation.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] ML[4:0] Attenuation** 0 00000 0 dB (Default) 0 00001 1.5 dB 0 11111 46.5 dB 1 xxxxx ∞ dB (Mute)
7:5			**Reserved.**
4:0	MR[4:0]	R/W	**Right Master Volume Control Attenuation.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] MR[4:0] Attenuation** 0 00000 0 dB (Default) 0 00001 1.5 dB 0 11111 46.5 dB 1 xxxxx ∞ dB (Mute)

4.1.3 Headphone Volume Register (Index 04h)

This register controls the Headphone output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphone Volume	Mute	x	x	ML4	ML3	ML2	ML1	ML0	x	x	x	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Headphone Master Volume Mute.** 0 = The channel volume is controlled by the ML[4:0] and MR[4:0] bits. 1 = The channel is muted. (Default.)
14:13			**Reserved.**
12:8	ML[4:0]	R/W	**Headphone Left Master Volume Control.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] ML[4:0] Attenuation** 0 00000 0 dB (Default) 0 00001 1.5 dB 0 11111 46.5 dB 1 xxxxx ∞ dB (Mute)
7:5			**Reserved.**
4:0	MR[4:0]	R/W	**Headphone Right Master Volume Control.** This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. **Mute [bit 15] MR[4:0] Attenuation** 0 00000 0 dB (Default) 0 00001 1.5 dB 0 11111 46.5 dB 1 xxxxx ∞ dB (Mute)

4.1.4 PC Beep Register (Index 0Ah)

This register controls the PC Beep input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0000h

Bit	Label	R/W	Description
15	Mute	R/W	**PC Beep Volume Mute.** 0 = The channel volume is unmuted (Default.) Because the PC Beep signal input to the audio mixer is used primarily for system diagnostic purposes, the default value for the PC Beep Volume is unmuted. 1 = The channel is muted.
14:0			**Reserved.**

4.1.5 Mic Volume Register (Index 0Eh)

This register controls the Mic input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	x	GN4	GN3	GN2	GN1	GN0	8008h

Bit	Label	R/W	Description
15	Mute	R/W	**Mic Volume Mute.** 0 = The channel volume is controlled by the GN[4:0] bits. 1 = The channel is muted. (Default.)
14:7			**Reserved.**
6	20dB	R/W	**Mic 20 dB Gain Enable.** 0 = Disable the Mic 20 dB boost. (Default.) 1 = Enable the Mic 20 dB boost.
5			**Reserved.**
4:0	GN[4:0]	R/W	**Mic Volume.** This field controls the Mic volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GN[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / –∞ dB (Mute)

4.1.6 Line In Volume Register (Index 10h)

This register controls the Line In input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**Line In Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left Line In Volume.** This field controls the Left Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GL[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / -∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right Line In Volume**. This field controls the Right Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] / GR[4:0] / Gain** 0 / 00000 / +12 dB 0 / 01000 / 0 dB (Default) 0 / 11111 / -34.5 dB 1 / xxxxx / -∞ dB (Mute)

4.1.7 CD Volume Register (Index 12h)

This register controls the CD input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**CD Volume Mute.** 1 = The channel is muted. (Default.) 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left CD Volume.** This field controls the Left CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GL[4:0] Gain** 0 00000 +12 dB 0 01000 0 dB (Default) 0 11111 -34.5 dB 1 xxxxx –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right CD Volume**. This field controls the Right CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GR[4:0] Gain** 0 00000 +12 dB 0 01000 0 dB (Default) 0 11111 -34.5 dB 1 xxxxx –∞ dB (Mute)

4.1.8 PCM Out Volume Register (Index 18h)

This register controls the PCM Out output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description
15	Mute	R/W	**PCM Out Volume Mute.** 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits. 1 = The channel is muted. (Default.)
14:13			**Reserved.**
12:8	GL[4:0]	R/W	**Left PCM Out Volume.** This field controls the Left PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GL[4:0] Gain** 0 00000 +12 dB 0 01000 0 dB (Default) 0 11111 -34.5 dB 1 xxxxx –∞ dB (Mute)
7:5			**Reserved.**
4:0	GR[4:0]	R/W	**Right PCM Out Volume**. This field controls the Right PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GR[4:0] Gain** 0 00000 +12 dB 0 01000 0 dB (Default) 0 11111 -34.5 dB 1 xxxxx –∞ dB (Mute)

4.1.9 Record Select Register (Index 1Ah)

This register selects the record source.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h

Bit	Label	R/W	Description
15:11			**Reserved.**
10:8	SL[2:0]	R/W	**Left Record Select.** This field selects the record source for the left channel. **SL[2:0] Left Record Source** 000 Mic (Default) 001 Left CD In 010 Not supported 011 Not supported 100 Left Line In 101 Left Stereo Mix 110 Mono Mix 111 PCM (implemented internally)
7:3			**Reserved.**
2:0	SR[2:0]	R/W	**Right Record Select.** This field selects the record source for the right channel. **SR[2:0] Right Record Source** 000 Mic (Default) 001 Right CD In 010 Not supported 011 Not supported 100 Right Line In 101 Right Stereo Mix 110 Mono Mix 111 PCM (implemented internally)

4.1.10 Record Gain Register (Index 1Ch)

This register controls the input record gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h

Bit	Label	R/W	Description
15	Mute	R/W	**Input Record Gain Mute.** 0 = Record gain is controlled by the GL[3:0] and GR[3:0] bits. 1 = The channel is muted. (Default.)
14:12			**Reserved.**
11:8	GL[3:0]	R/W	**Left Input Record Gain.** This field controls the Left Input Record Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GL[3:0] Gain** 0 1111 +22.5 dB 0 0000 0 dB (Default) 1 xxxxx –∞ dB (Mute)
7:4			**Reserved.**
3:0	GR[3:0]	R/W	**Right Input Record Gain.** This field controls the Right Input Record Gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. **Mute [bit 15] GR[3:0] Gain** 0 1111 +22.5 dB 0 0000 0 dB (Default) 1 xxxxx –∞ dB (Mute)

4.1.11 General Purpose Register (Index 20h)

This register controls the local loopback function. This register should be read before writing, to generate a mask for only the bit(s) that need to be changed.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	x	x	x	x	x	x	x	x	LPBK	x	x	x	x	x	x	x	0000h

Bit	Label	R/W	Description
15:8			**Reserved.**
7	LPBK	R/W	**ADC/DAC Loopback Mode Enable.** 0 = Disable loopback. (Default.) 1 = Enable loopback of the stereo ADC output to the stereo DAC input (left-to-left, right-to-right) without involving the AC-link, allowing for full system performance measurements.
6:0			**Reserved.**

4.1.12 Powerdown Control/Status Register (Index 26h)

This register controls powerdown states and monitors subsystem readiness. The lower four bits are read-only status with a "1" indicating that the subsection is "ready". Ready indicates the subsection is able to perform in its nominal state. When this register is written, the bit values that come in on AC-link have no effect on read only bits 4-0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Powerdown Control/Status	x	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	x	PDA	x	**REF**	**ANL**	**DAC**	**ADC**	400xh

Bit	Label	R/W	Description
15			**Reserved.**
14	PR6	R/W	**Powerdown Headphone Amplifier.** 0 = Do not powerdown Headphone Amplifier. 1 = Powerdown Headphone Amplifier. (Default.)
13	PR5	R/W	**Powerdown Internal Clock Circuit.** 0 = Do not powerdown internal clock circuit. (Default.) 1 = Powerdown internal clock circuit.
12	PR4	R/W	**Powerdown Digital Interface.** 0 = Do not powerdown digital AC-link interface. (Default.) 1 = Powerdown digital AC-link interface.
11	PR3	R/W	**Powerdown Analog Mixer with Vref Off.** PR3 can be used in combination with PR2 or by itself. 0 = Do not powerdown Analog Mixer. (Default.) 1 = Powerdown Analog Mixer and turn Vref off.
10	PR2	R/W	**Powerdown Analog Mixer with Vref On.** 0 = Do not powerdown Analog Mixer. (Default.) 1 = Powerdown Analog Mixer but leave Vref on.
9	PR1	R/W	**Powerdown PCM Output DACs.** 0 = Do not powerdown PCM Output DACs. (Default.) 1 = Powerdown PCM Output DACs.
8	PR0	R/W	**Powerdown PCM Input ADCs and Input Mux.** 0 = Do not powerdown PCM Input ADCs and Input Mux. (Default.) 1 = Powerdown PCM Input ADCs and Input Mux.
7	PRZ	R/W	**Powerdown Clock Interface Except BIT_CLK.** 0 = Do not powerdown Clock Interface. (Default.) 1 = Powerdown Clock Interface except BIT_CLK output. This turns off all digital power to clock interface except BIT_CLK so the ASIC controller can monitor GPIOs.
6			**Reserved.**
5	PDA	R/W	**Powerdown Line Out Amplifiers.** 0 = Do not powerdown stereo Line Out output amplifiers. (Default.) 1 = Powerdown stereo Line Out output amplifiers (left and right).
4			**Reserved.**
3	REF	R	**Audio Reference Voltages Ready Status.** 0 = Audio reference voltages (Vrefs) not ready. 1 = Audio reference voltages (Vrefs) ready (at nominal level).
2	ANL	R	**Analog Mixers Ready Status.** 0 = Analog mixers not ready. 1 = Analog mixers ready.
1	DAC	R	**DAC Ready Status.** 0 = Stereo playback DAC not ready to accept data. 1 = Stereo playback DAC ready to accept data.
0	ADC	R	**ADC Ready Status.** 0 = Stereo record ADC not ready to transmit data. 1 = Stereo record ADC ready to transmit data.

4.1.13 Extended Audio ID Register (Index 28h)

The read-only Extended Audio ID register identifies which extended audio features are supported (in addition to the original AC '97 features identified by reading the Reset register at Index 0h). A non-zero Extended Audio ID register value indicates one or more of the extended audio features is supported. ID0 and ID1 will reflect the state of the external codec ID pins as well as the detection of the PRIMARY_DN signal.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	**ID1**	**ID0**	x	x	x	x	**AMAP**	**LADC**	**SDAC**	**CDAC**	x	x	**VRM**	x	**DRA**	**VRA**	x201h

Bit	Label	R/W	Description
15:14	ID[1:0]	R	**Codec Configuration Identifier.** This 2-bit field identifies the codec configuration. ID0 and ID1 reflect the state of the external codec ID pins as well as the detection of the PRIMARY_DN signal. 00 = Primary codec configuration supported. 01, 10, or 11 = Secondary codec configuration supported.
13:10			**Reserved.**
9	AMAP	R	**Default Audio Mapping Support.** 0 = Not supported. 1 = Supported. (Default.)
8	LDAC	R	**PCM LFE DAC.** 0 = Not supported. (Default.) 1 = Supported.
7	SDAC	R	**PCM Surround DAC.** 0 = Not supported. (Default.) 1 = Supported.
6	CDAC	R	**PCM Center DAC.** 0 = Not supported. (Default.) 1 = Supported.
6:4			**Reserved.**
3	VRM	R	**Variable Rate Mic Supported** 0 = Not supported. (Default.) 1 = Supported.
2			**Reserved.**
1	DRA	R	**Double Rate PCM Audio.** 0 = Not supported. (Default.) 1 = Supported.
0	VRA	R	**Variable Rate PCM Audio Supported** 0 = Not supported 1 = Supported. (Default.)

4.1.14 Extended Audio Status and Control Register (Index 2Ah)

The Extended Audio Status and Control Register provides status and control of the extended audio features.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Extended Audio Status/Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	VRA	0000h

Bit	Label	R/W	Description
15:1			**Reserved.**
0	VRA	R/W	**Variable Rate PCM Audio Mode Enable.** 0 = Disables Variable Rate PCM Audio Mode. (Default.) 1 = Enables Variable Rate PCM Audio Mode.

4.1.15 PCM Front DAC Rate Control Register (Index 2Ch)

Read/write registers 2Ch (PCM Front DAC Rate) and 32h (PCM LR ADC Rate) operate in a similar manner. Writing to these audio sample rate control registers alters the DAC and ADC rate for those channels.

Register 2Ch controls the PCM Front DAC sample rate.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**PCM Front DAC Sample Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2B11 — 11.025 kHz 2EE0 — 12 kHz 3E80 — 16 kHz 5622 — 22.050 kHz 5DC0 — 24 kHz 7D00 — 32 kHz AC44 — 44.1 kHz BB80 — 48 kHz (Default.)

4.1.16 PCM LR ADC Rate Control Register (Index 32h)

Register 32h controls the PCM LR ADC sample rate.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**PCM LR ADC Rate.** 16-bit unsigned value as follows: **D[15:0] (hex) — Sample Rate** 1F40 — 8 kHz 2B11 — 11.025 kHz 2EE0 — 12 kHz 3E80 — 16 kHz 5622 — 22.050 kHz 5DC0 — 24 kHz 7D00 — 32 kHz AC44 — 44.1 kHz BB80 — 48 kHz (Default.)

4.1.17 Extended Modem ID Register (Index 3Ch)

Read-only register 3Ch primarily identifies the codec's modem capabilities.

Even though the bits are listed as read only, the register is actually a read/write register. Writing any value to this register performs a register reset, which causes all modem-related registers to revert to their default values.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	CID2	CID1	HSET	LIN2	LIN1	x001h

Bit	Label	R/W	Description
15:14	ID[1:0]	R	**Codec Configuration Identifier.** This 2-bit field identifies the codec configuration. ID0 and ID1 reflect the state of the external codec ID pins as well as the detection of the PRIMARY_DN signal (see Table 3-2). 00 = Primary codec configuration. 01, 10, or 11 = Secondary codec configuration.
13:5			**Reserved.**
4	CID2	R	**Caller ID Decode for Line 2 Supported.** 0 = Not supported. (Default.) 1 = Supported.
3	CID1	R	**Caller ID Decode for Line 1 Supported.** 0 = Not supported. (Default.) 1 = Supported.
2	HSET	R	**Handset DAC.** 0 = Not supported. (Default.) 1 = Supported.
1	LIN2	R	**Line 2 Supported.** 0 = Not supported. (Default.) 1 = Supported.
0	LIN1	R	**Line 1 Supported.** 0 = Not supported. 1 = Supported. (Default.)

4.1.18 Extended Modem Status and Control Register (Index 3Eh)

This register controls GPIO powerdown and reports GPIO ready status. This register functions similarly to the Powerdown Control/Status (register 26h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Eh	Extended Modem Status/Control	x	x	x	x	x	x	x	PRA	x	x	x	x	x	x	x	GPIO	010xh

Bit	Label	R/W	Description
15:9			**Reserved.**
8	PRA	R/W	**Powerdown GPIO.** 0 = Do not powerdown GPIO. 1 = Powerdown GPIO (including the wake-up event logic). (Default.) **NOTE:** When the GPIO section is powered down, all outputs are three-stated and input slot 12 is marked invalid when the AC-link is active.
7:1			**Reserved.**
0	GPIO	R	**GPIO Ready Status.** 0 = Not ready. (Default.) 1 = Ready.

4.1.19 Modem Line 1 ADC/DAC Rate Control Register (Index 40h)

Since modem sample rate is fixed at a 16 kHz and is controlled by LSD, this register has no effect on the true sample rate of ADC/DAC data. If a value other than the sample rates shown in the following table is written by the host, the sample rate register value will automatically revert to the default sample rate of 48 kHz (BB80h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Modem Line 1 ADC/DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description
15:0	SR[15:0]	R/W	**Modem Line 1 ADC/DAC Sample Rate.** 16-bit unsigned value between 0 and 65535 as follows representing the rate of operation in Hz: **D[15-0] (hex) — Sample Rate** 1F40 — 8 kHz 2580 — 9.6 kHz 3592 — 13.71428 kHz 3E80 — 16 kHz 4B00 — 19.2 kHz 5DC0 — 24 kHz BB80 — 48 kHz (Default.)

4.1.20 GPIO Pin Configuration Register (Index 4Ch)

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

On reset (Cold or Warm), all pins are configured as inputs.

The status of all implemented GPIO pins (4 and 5) will initially read back “1” (via Slot 12 or register 54h). Unimplemented GPIO pins will always read back 0. This scheme informs software as to how many GPIO pins have been implemented. The controller must send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ch	GPIO Pin Configuration	x	x	x	x	x	x	x	x	x	x	GC5	GC4	x	x	x	x	0030h

4.1.21 GPIO Pin Polarity/Type Register (Index 4Eh)

The GPIO Pin Polarity/Type is a read/write register that defines:

- GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an input.
- GPIO Output Type (0=CMOS, 1=Open-drain) when a GPIO pin is configured as an output.

On reset (Cold or Warm), this register defaults to all 1s.

An unimplemented GPIO pin always returns a 1.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Eh	GPIO Pin Polarity/Type	x	x	x	x	x	x	x	x	x	x	GP5	GP4	x	x	x	x	FFFFh

4.1.22 GPIO Pin Sticky Register (Index 50h)

The GPIO Pin Sticky read/write register defines GPIO Input Type (0 = Not Sticky, 1 = Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of the GPIO Pin Status register 54h and by reset.

On reset (Cold or Warm), this register defaults to all 0s specifying Non-Sticky.

An unimplemented GPIO pin always returns a 0.

Sticky is defined as edge sensitive; Non-Sticky is defined as level sensitive.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
50h	GPIO Pin Sticky	x	x	x	x	x	x	x	x	x	x	GS5	GS4	x	x	x	x	0000h

4.1.23 GPIO Pin Wake up Mask Register (Index 52h)

The GPIO Pin Wake up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake up or GPIO_INT (0 = No, 1 = Yes). When the AC-link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wake up event will trigger the assertion of SDATA_IN (the AC-link wake up protocol is defined in another section of this document). When the AC-link is powered up, a wake up event will appear as GPIO_INT=1 on bit 0 of input slot 12.

An AC-link wake up Interrupt is defined as a 0-to-1 transition on SDATA_IN when the AC-link is Powered down (Register 26h PR4=1). GPIO bits that have been programmed as Inputs, Sticky and Pin Wake up, upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-link wake up event (transition of SDATA_IN from "0 to 1), if and only if the AC-link was powered down.

On reset (Cold or Warm) this register defaults to all 0s specifying no wake up event.

Unimplemented GPIO pins always returns 0s.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
52h	GPIO Pin Wake up	x	x	x	x	x	x	x	x	x	x	GW5	GW4	x	x	x	x	0000h

4.1.24 GPIO Pin Status Register (Index 54h)

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this register.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12.

Reset does not affect the value read. It is always the state of the GPIO pin. GPIO bits that have been programmed as Inputs and Sticky, upon transition either (high-to-low) or (low-to-high) depending on Pin polarity, will cause the individual GI bit to go set to a 1, and remain set until a write of 0 to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12. (See Table 5-1.)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	GPIO Pin Status	x	x	x	x	x	x	x	x	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	00xxh

4.1.25 Miscellaneous Modem Register (Index 56h)

This purpose of this register is to control additional modem functions.

The only bit used in this register is MLNK, which was supposed to be set in order to have SDATA_IN asserted when attempting to wake-up the AC-link. This function is not required and is not supported. However, this bit has been physically implemented in order to use it in future revisions.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Misc Modem AFE Status/Control	x	x	x	MLNK	x	x	x	x	x	x	x	x	x	x	x	x	0000h

Bit	Label	R/W	Description
15:13			**Reserved.**
12	MLNK	R/W	**MC '97 Link.** Controls MC '97 AC-link status. Not supported. Bit state has no effect. 0 = AC-link is on (active). (Default.) 1 = AC-link is off (sleep).
11:0			**Reserved.**

4.1.26 Mixer Volume Register (Index 5Ah)

This register controls the attenuation on each of the signals coming into the main mixer so as to prevent clipping of the final signal. The step size is 1.5 dB and the range is 0 to –22.5.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah	Mixer Volume	x	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h

Bit	Label	R/W	Description
15:12			**Reserved.**
11:8	MXL[3:0]	R/W	**Left Mixer Volume Attenuation**. This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. **MXL[3:0] Attenuation** 0000 0 dB (Default) 0001 1.5 dB …. …. 1111 22.5 dB
7:4			**Reserved.**
3:0	MXR[3:0]	R/W	**Right Mixer Volume Attenuation.** This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. **MXR[3:0] Attenuation** 0000 0 dB (Default) 0001 1.5 dB …. …. 1111 22.5 dB

4.1.27 Miscellaneous Audio Register (Index 5Ch)

This register allocates bits to control SPDIF output, select audio slot/DAC mapping, and route Microphone data to AC-link slot 6. Bit 8 is designated to control the powerdown of Mic Bias.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ch	Miscellaneous Audio	x	x	x	x	x	MuteLvl	PdLvl	PdMicB	x	MicSel	DacSel1	DacSel0	SPDifEn	CpRight	Mode1	Mode0	0600h

Bit	Label	R/W	Description
15:11			**Reserved.**
10	MuteLvl	R/W	**Mute True Line Level.** Controls muting of true line level output driver. 0 = Not muted. 1 = Muted. (Default.)
9	PdLvl	R/W	**Powerdown True Line Level.** Controls power down of true line level output driver. 0 = Powered up. 1 = Powered down. (Default.)
8	PdMicB	R/W	**Powerdown Mic Bias.** Controls power down of the mic bias. 0 = Powered up. (Default.) 1 = Powered down.
7			**Reserved.**
6	MicSel	R/W	**Mic Select.** Controls routing of ADC Mic data to AC-link slot 6. 0 = Disabled. (Default.) 1 = Enabled.
5:4	DacSel	R/W	**DAC Select.** Controls DAC channel support. 00 = Default (based on codec_id). 01 = Force front channel. 10 = Force rear channel. 11 = Force center/LFE channel.
3	SPDifEn	R/W	**SPDIF Powerdown Enable.** Controls powerdown of SPDIF output. 0 = Disabled. (Default.) 1 = Enabled.
2	CpRight	R/W	**Copy Right Control for SPDIF**. Controls setting of the copy right bit for the SPDIF output. 0 = Copying not allowed. (Default.) 1= Copying allowed.
1:0	Mode	R/W	**Mode Select.** Controls SPDIF mode. 0X = Linear PCM consumer mode (Default = 00.) 10 = AC-3 bit-stream consumer mode 11 = Invalid

4.1.28 DIB Control (Index 66h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	DIB Control	x	**DRDB1**	x	INTE1	x	**RG1**	x	**RGIE1**	x	x	PDDXE	CTBSY	IRAR	x	PDX	x	x00xh

Bit	Label	R/W	Description
15			**Reserved.**
14	DRDB1	R	**DIB Ready Status.** Indicates status of DIB interface. 0= DIB is busy. 1= DIB is ready.
13			**Reserved.**
12	INTE1	R/W	**DIB Ready Interrupt Enable.** Controls enabling of GPIO interrupt to host based on DRDB1 transition from 0 to 1. Causes GPIO7, when configured for an input, to reflect the status of DRDB1. 0 = Disable. (Default.) 1 = Enable.
11			**Reserved.**
10	RG1	R	**Ring Good Status.** Indicates ring qualification. 0 = Ring qualified as bad. 1 = Ring qualified as good.
9			**Reserved.**
8	RGIE1	R/W	**Ring Good Interrupt Enable.** Controls enabling GPIO interrupt to host based on RG1 transition from 0 to 1. 0 = Disable. (Default.) 1 = Enable.
7:6			**Reserved.**
5	PDDXE	R/W	**Crystal Circuit Powerdown Enable in Power Down Mode.** Controls enabling of crystal circuit power down in power down mode. 0 = Disable. (Default.) 1 = Enable.
4	CTBSY	R	**Counter Busy Status**. Indicates the expiration status of the CID Time Out counter in register 6A that switches from RC oscillator to using BIT_CLK. When busy, the counter is being incremented and the HSD registers are not accessible through the AC-link interface. Reset automatically by the CX20468. 0 = Counter has not expired. (Default.) 1 = Counter has expired.
3	IRAR	R/W	**Indirect Read Automatic Return Enable.** Controls enabling of Indirect Read Automatic Return. When enabled, if the host issues a write to the indirect register that requests a read of the HSD/LSD, the data is automatically returned as if an AC-link read request was issued. 0 = Disable. (Default.) 1 = Enable
2			**Reserved.**
1	PDX	R/W	**Crystal Circuit Power Down Enable.** Controls crystal circuit power-down enable. 0 = Power up (default for primary). 1 = Power down (default for secondary).
0			**Reserved.**

4.1.29 Cold Reset Mask (Index 68h)

The cold reset mask allows certain sections to NOT be reset when the masked value is written before the SmartAMC goes into sleep mode. Register banks are preserved with their original values. E8B4h is the 16-bit decode value that needs to be written in order for cold reset masking to be enabled.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	Cold Reset Mask	CMR15	CMR14	CMR13	CMR12	CMR11	CMR10	CMR9	CMR8	CMR7	CMR6	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	xxxxh

Bit	Label	R/W	Description
15:0	CMR	R/W	**Cold Reset Mask.** Controls the cold reset mask. E8B4h = Masked Others = Not masked

4.1.30 CID Time Out (Index 6Ah)

Register 6Ah contains a CID Time Out timer.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	CID Time Out	x	x	x	x	x	x	x	x	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	0040h

Bit	Label	R/W	Description
15:6			**Reserved.**
7:0	CT	R/W	**CID Time Out**. This timer is used to determine when to switch from the crystal to using BIT-CLK after ring qualification completes while in Secondary Mode. Each count is approximately 42.66 ms in duration. The register defaults to 0040h, which is about a 2.73 second delay. It does not need to be re-programmed again unless a cold reset occurs. However, the assertion of RESET# will not affect this register if the cold reset mask register is enabled. The CTBSY status bit, located at 66:4, indicates to the software when the counter is busy.

4.1.31 Indexed1 Register (Index 7Ah)

The Indexed1 Register is a multipurpose register used to access the Host Side Device (HSD) and Line Side Device (LSD) register set.

The HSD space is mapped to index registers 00h to 3Fh.

The LSD space is mapped to index registers 40h to 7Fh.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	Indexed1 Register	IRWB	IADDR6	IADDR5	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	**IDAT7**	**IDAT6**	**IDAT5**	**IDAT4**	**IDAT3**	**IDAT2**	**IDAT1**	**IDAT0**	80xxh

Bit	Label	R/W	Description
15	IRWB	R/W	**Read/Write.** 0 = Write 1 = Read (Default.)
14:8	IADDR [6:0]	R/W	**Indexed Register Address.** (Default 0.)
7:0	IDAT [7:0]	R/W	**Indexed Register Data.** (Default 0.)

4.1.32 Vendor ID Registers 1 and 2 (Indexes 7Ch and 7Eh)

This register contains the vendor identification code and revision numbers.

The vendor identification code is reported in the F[7:0], S[7:0], and T[7:0] fields. The ID method is Microsoft's Plug and Play Vendor ID code.

The vendor revision number is reported in the REV[7:0] field.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4358h

Bit	Label	R/W	Description
15:8	F[7:0]	R	**Vendor ID Code Character 1.** Conexant ID code character 1: ASCII "C" (43h).
7:0	S[7:0]	R	**Vendor ID Code Character 2.** Conexant ID code character 2: ASCII "X" (58h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5428h

Bit	Label	R/W	Description
15:8	T[7:0]	R	**Vendor ID Code Character 3.** Conexant ID code character 3: ASCII "T" (54h).
7:0	REV[7:0]	R	**Vendor Revision Number**. Revision number. The initial number is 28h.

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5 Digital Interface

The codec communicates with the controller via a digital serial link (AC-link). All digital audio streams, modem line codec stream, handset, GPIO, and command/status information is transferred between the controller and the codec over this point to point serial channel. The AC-link interface signals are shown in Figure 5-1 and are described in Table 5-1.

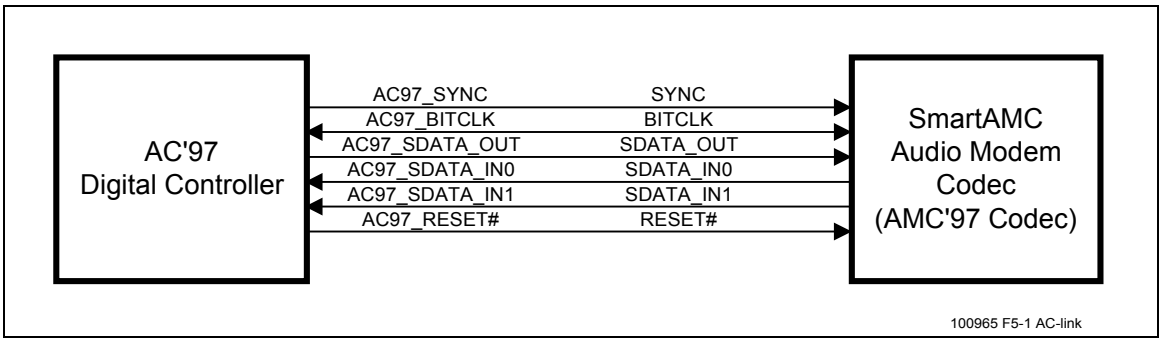

Figure 5-1. AMC '97 Codec Connection to AC '97 Controller

Table 5-1. AC-link Serial Interface Signals

Signal Name	MC I/O	Description
SYNC	I	48 kHz fixed rate sample synchronization from the controller to the codec.
BIT_CLK	I O	12.288 MHz serial data clock to the codec (Secondary AMC). 12.288 MHz serial data clock from the codec (Primary AMC).
SDATA_IN0	O	Serial data stream from the codec to the controller (Primary AMC).
SDATA_IN1	O	Serial data stream from the codec to the controller (Secondary AMC).
SDATA_OUT	I	Serial data stream from the controller to the codec.
RESET#	I	Master hardware reset from the controller

The control and status slots allow writing and reading of registers internal to the SmartAMC. These 16-bit registers are addressed at word-aligned byte addresses 0x00, 0x02, 0x04, …, 0x7E. Registers 0x00 - 0x58 are predefined, 0x5A - 0x7A are reserved for the vendor, 0x7C and 0x7E are for the vendor ID.

Because provisions exist for the modem and other sample rates to be less than 48 kHz, the TAG slot contains bits which indicate the validity of each slot in the serial stream.

The AC '97 specification also defines slot request bits that allow the codec to request samples from the controller. These bit definitions (active low) are implemented as defined in that specification.

When a slot is valid for the outgoing stream, the controller places a one in the corresponding bit position in the TAG slot. For all slots other than the PCM left and right slots, the codec ignores the data present in the slot when the slot's tag bit is a 0 for that particular data phase. This allows the controller to simply repeat the current sample if desired. However, the controller must respond properly to the SLOTREQ bits. For the PCM left and right slots, the codec assumes every slot is valid. If the slot is invalid, the controller must send 0's for the data.

When a slot is valid for the incoming stream, the codec places a one in the corresponding bit position in the TAG slot. The controller must ignore the data present in the slot when the slot's tag bit is a 0 for that particular data phase. The Codec puts zeros in the slot when the slot is invalid.

The AC-link request for status always returns in the next frame. The request is, therefore, always delayed by one frame time. A write request in the current frame will not affect the status that is returned in that particular write frame. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the controller.

The time slots supported by the SmartAMC are listed in Table 5-2.

Table 5-2. SmartAMC Supported Slot Assignments

Slot Number	SDATAOUT (Controller to AMC)	SDATAIN (AMC to Controller)
0	TAG	TAG
1	Command Address Port	Status Address Port
2	Command Data Port	Status Data Port
3	PCM Playback Left Channel	PCM Record Left Channel
4	PCM Playback Right Channel	PCM Record Right Channel
5	Modem Line 1 DAC Input Data	Modem Line 1 ADC Output Data
6	PCM Center Channel	Mic ADC Output Data
7	PCM Left Surround Channel	Not Supported
8	PCM Right Surround Channel	Not Supported
9	PCM LFE Channel	Not Supported
10	Not Supported	Not Supported
11	Not Supported	Not Supported
12	GPIO Control	GPIO Status

5.1 SDATA_IN (Codec to Controller) Slot Definitions

5.1.1 Input Slot 1: Status Address Port / SLOTREQ Bits

Slot 1, the Status Address Port, delivers codec control register read address slot request flags for all output slots.

The Slot 1 tag bit is independent of the bit 11:2 slot request field, and **only** indicates valid Status Address Port data (Control Register Index). The AMC sets SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to "1" when returning valid data from a previous register read. They are otherwise set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots are driven with 0s for maximum compatibility with the original AC '97 Component Specification. Output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit is forced to “1” in the interval between when the powerdown bit for its associated channel is turned off and when its channel is ready to accept samples. The controller can take advantage of this scheme to eliminate the need to poll the AMC status registers.

To power down a channel, the controller needs only to:

1. Disable the source of DAC samples in controller.
2. Use the powerdown control/status bits in HSD registers 26h, 3Eh, 5Ch, and LSD registers.

To power up a channel, the controller needs only to:

1. Use the powerdown control/status bits in HSD registers 26h, 3Eh, 5Ch, and LSD registers
2. Enable the source of DAC samples in controller.

Variable Sample Rate Signaling Protocol

For variable sample rate output, the codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame signal which *active output slots* require data from the controller in the next audio output frame. An *active output slot* is defined as any slot supported by the codec that is not in a powerdown state. For fixed 48 kHz operation, the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

Upon reset, the audio sample rate registers default to 48 kHz.

5.1.2 Input Slot 2: Status Data Port

Input Slot 2, the Status Data Port, port delivers 16-bit control register read data.

Input Slot 2: Status Data Port	
Bit	**Description**
19:4	**Control Register Read Data.** Stuffed with 0’s if tagged “invalid” by the codec.
3:0	**Reserved.** Stuffed with 0’s by the codec.

5.1.3 Input Slot 3: PCM Left Record Data

Input Slot 3 contains the 18-bit PCM left channel ADC output data.

Input Slot 3: PCM Left Channel ADC Output Data	
Bit	**Description**
19:2	**PCM Left Channel ADC Output Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Not Used.** Stuffed to 0’s by the codec.

5.1.4 Input Slot 4: PCM Right Record Data

Input Slot 4 contains the 18-bit PCM right channel ADC output data.

Input Slot 4: PCM Right Channel ADC Output Data	
Bit	**Description**
19:2	**PCM Right Channel ADC Output Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Not Used.** Stuffed to 0's by the codec.

5.1.5 Input Slot 5: Modem Line 1 ADC Output Data

Input Slot 5 contains the 16-bit Modem Line 1 ADC output data.

Operates as a single line Data/Fax/Voice/TAM only modem only AC'97 rev 2.1 compatible codec with the Line Side Device and DIB (uses slot 5 and 12).

Input Slot 5: Modem Line 1 ADC Output Data	
Bit	**Description**
19:4	**Modem Line 1 ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

5.1.6 Input Slot 6: Microphone ADC Output Data

Input Slot 6 contains the 16-bit Microphone ADC output data.

Input Slot 6: Microphone ADC Output Data	
Bit	**Description**
19:4	**Microphone ADC Output Data.** 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	**Not Used.** Stuffed to 0's by the codec.

The SmartAMC shares the PCM ADC with the MIC and other inputs (see Figure 1-4). Upon power on, ADC MIC data is automatically routed to AC-link input slot 3 and 4. However, this data can also be routed to slot 6 by setting MicSel bit (see Table 5-3).

Table 5-3: Mapping ADC Mic Data to AC-link Slots

Select to Record (1Ah)	MicSel (56h[6])	AC-link Slot Mappings
Mic	0	3 and 4
Mic	1	3, 4, and 6

5.1.7 Input Slots 7-11: Reserved

Input Slots 7-11 are reserved.

Input Slot 7-11: Reserved	
Bit	**Description**
19:0	Stuffed to 0's by the codec.

5.1.8 Input Slot 12: GPIO Status

Input Slot 12 contains the GPIO status bits (Table 5-4). The codec constantly updates the status slot based upon the logic level detected at each GPIO configured for input. The controller must debounce the reported states as required for the 48 kHz sample rate.

By default, the GPIO power-down bit (bit 8 of register 3Eh) is set. This bit must be cleared upon power up.

Only two (bit 5:4) of the eight (bits 7:0) GPIO bits defined for AC-link are implemented on the CX20468 HSD. The other GPIs are implemented in the CX20463 LSD.

GPI0-GPI2 (internal to LSD) are mapped to LCL (Line Current Loss) for monitoring line connection, RDO (Ring Detect Output) and RDOB (Ring Detect Output Bar) for detecting ring respectively. These are all inputs from the CX20463 LSD and configurable to interrupt/wake-up the CX20468 HSD through the DIB. The remaining GPIOs are also mapped to the LSD register space.

All GPIOs present their status over slot 12 of the SDATA_IN signal. The HSD logic default operation (when the software has NOT requested a DIB transfer) is to read the LSD GPIO pin status register low (GPIOS_L). This information is constantly reflected into slot 12 of SDATA_IN. Since the CX20468 HSD supports only eight GPIO bits, it does not use all the 16 GPIO status bit available in slot 12. The unused bits are forced to 0. Additionally, the upper two bits (7:6) may be replaced with alternate, interrupt related functionality, as described:

- When the INTE1 bit is set (bit 12 of register 66h), GPIO7 is logically connected to the DRDB1 bit (bit 14 of register 66h).
- When the RGIE1 bit is set (bit 8 of register 66h), GPIO6 is logically connected to the RG1 bit (bit 10 of register 66h).

Table 5-4. AC-link GPIO Mapping

GPIO-Slot-bit	INTE1 (66h:12)	RGIE1 (66h:8)	GPIO source
19-12			N/A (stuffed with zeros)
11	0 (default)		External GPIO2 LSD function (GPIO7 = Pin 1, labeled GPIO2)
11	1		'dib_ready'
10		0 (default)	External GPIO1 LSD function (GPIO6 = Pin 32, labeled GPIO1)
10		1	Internal ring qualification (Ring_good)
9			GPIO5
8			GPIO4
7			Internal LSD function (GPI3 = NA)
6			Internal LSD function (GPI2 = RDOB)
5			Internal LSD function (GPI1 = RDO)
4			Internal LSD function (GPI0 = LCL)
3-1			N/A
0			Interrupt

5.2 SDATA_OUT (Controller to Codec) Slot Definitions

For playback, in both Primary and Secondary modes, Digital PCM Stereo out data can be routed by the controller for stereo DAC conversion to:

- PCM L & R slots (AC-link slots 3 and 4), typically used for Front Speakers
- PCM L & R Surround slots (AC-link slots 7 and 8), typically used for Surround Speakers
- PCM Center & LFE slots (AC-link slots 6 and 9), typically used for Subwoofer and Center Speakers

The AMAP bit (bit 9 of register 28h) indicates that the CX20468 HSD supports optional AC-link output slots to audio DAC mapping. Upon power on, depending on the device ID, the codec slots to DAC mapping is defined as shown in Table 5-5. However, in both primary and secondary configurations, the mapping of AC-link PCM output slots to the device's 2-channel audio DAC function can be manipulated by setting DacSel bits (register 5Ch).

Table 5-5. PCM Output Slots to DAC Mappings in Default

Codec ID	AC-link Frame Data Used for Stereo DAC		Description
	PCM Left DAC uses data from Slot No.	PCM Right DAC uses data from Slot No.	
00	3	4	PCM L and R slots
01	3	4	PCM L and R slots
10	7	8	PCM L and R surround slots
11	6	9	PCM Center and LFE slots

5.2.1 Output Slot 1: Command Address Port

Output Slot 1, the Command Address Port, is used to control features and monitor status (see Input Slots 1 and 2) for codec functions such as mixer settings and power management.

Output Slot 1: Command Address Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

5.2.2 Output Slot 2: Command Data Port

Output Slot 2, the Command Data Port, is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19). If the current command port operation is a read, then the entire slot time must be stuffed with 0's by the controller.

Output Slot 2: Command Data Port	
Bit	**Description**
19	**Read/Write Command.** 1 = Read; 0 = Write.
18:12	**Control Register Index.** 64 16-bit locations, addressed on even byte boundaries.
11:0	**Not Used.** Stuffed to 0's by the controller.

5.2.3 Output Slot 3: PCM Left Playback Data

Output Slot 3 contains the 18-bit PCM left channel DAC input data.

Output Slot 3: PCM Left Channel DAC Input Data	
Bit	**Description**
19:2	**PCM Left Channel DAC Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.4 Output Slot 4: PCM Right Playback Data

Output Slot 4 contains the 18-bit PCM right channel DAC input data.

Output Slot 4: PCM Right Channel DAC Input Data	
Bit	**Description**
19:2	**PCM Right Channel DAC Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.5 Output Slot 5: Modem Line 1 DAC Input Data

Output Slot 5 contains the 16-bit Modem Line 1 DAC input data.

Output Slot 5: Modem Line 1 DAC Input Data	
Bit	**Description**
19:4	**Modem Line 1 DAC Input Data.** 16-bit sample (bit 19 = MSD; bit 4 = LSD)
3:0	**Not Used.** Stuffed to 0's by the controller.

5.2.6 Output Slot 6: PCM Center Channel

Output Slot 6 contains the PCM Center Channel input data.

Output Slot 6: PCM Center Channel Input Data.	
Bit	**Description**
19:2	**PCM Center Channel Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.7 Output Slot 7: PCM Left Surround Channel

Output Slot 7 contains the PCM Left Surround Channel input data.

Output Slot 7: PCM Left Surround Channel Input Data.	
Bit	**Description**
19:2	**PCM Left Surround Channel Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.8 Output Slot 8: PCM Right Surround Channel

Output Slot 8 contains the PCM Right Surround Channel input data.

Output Slot 8: PCM Right Surround Channel Input Data.	
Bit	**Description**
19:2	**PCM Left Surround Channel Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.9 Output Slot 9: PCM LFE Channel

Output Slot 9 contains the PCM LFE channel input data.

Output Slot 9: PCM LFE Channel Input Data.	
Bit	**Description**
19:2	**PCM LFE Channel Input Data.** 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	**Control Register Index.** Stuffed to 0's by the controller.

5.2.10 Output Slots 10-11: Reserved

Output Slots 10-11 are reserved.

Output Slot 10-11: Reserved	
Bit	**Description**
19:0	**Reserved.** Stuffed to 0's by the controller.

5.2.11 Output Slot 12: GPIO Control

Output Slot 12 contains the GPIO control bits. The codec constantly sets the GPIOs that are configured for output based upon the value of the corresponding bit position of the control slot.

5.3 General Purpose Inputs/Outputs

The Codec contains a number of General Purpose Input/Outputs suitable for easy connection with minimal parts to a DAA circuit. The controller must configure any GPIOs as outputs on power-up.

When configured as an input, a GPIO performs as a CMOS Schmitt triggered input for a 3.3V power supply. The board designers are responsible for connecting unused pins to VDD or VSS. However, to prevent excess power loss due to floating conditions during an extended reset period, all GPIOs, when RESET# is asserted, are pulled down.

The GPIOs are three-stated to a high impedance state on power-on or a cold reset. The controller must first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs have slow rise and fall times. Typical values should be 40 ns. In addition, the device sinks 2.4 mA at a maximum level of 0.4V and sources 2.4 mA at a minimum level of 2.97V.

Upon a warm reset, the GPIOs that are configured for outputs maintain their output values. As long as the controller does not tag the GPIO control slot as valid, the outputs will not change.

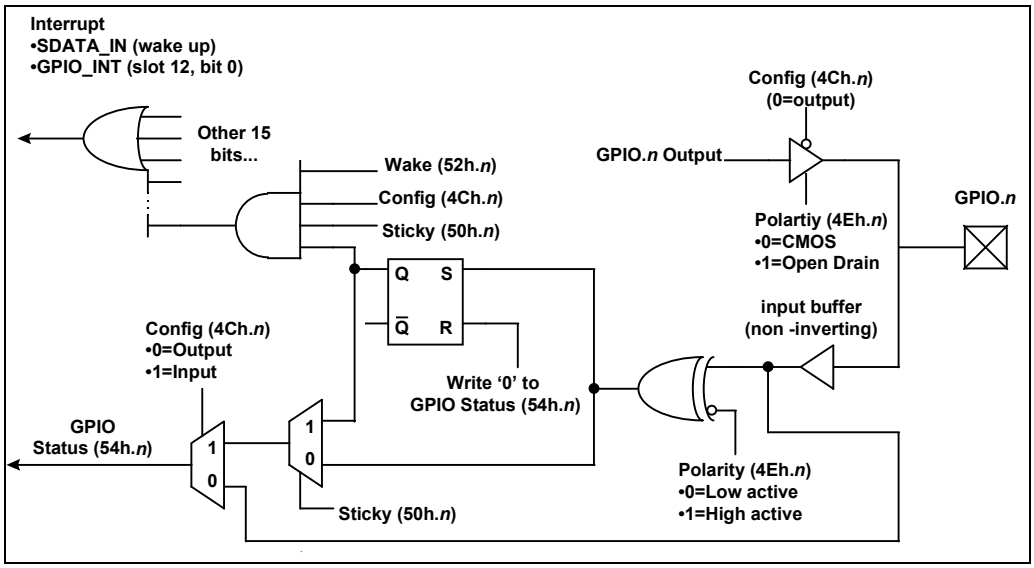

Figure 5-2. Conceptual GPIO Configuration

5.4 Low Power Modes

The Codec is a fully static design, i.e., when the clock is stopped to any subsection of the device, that subsection maintains its value.

The low power modes specified in Section 7 of the AC '97 Specification are supported, i.e., the modem ADC/DAC and the audio ADC/DAC can be individually powered down and up. See the Powerdown Control/Status and the Modem Powerdown Control/Status registers.

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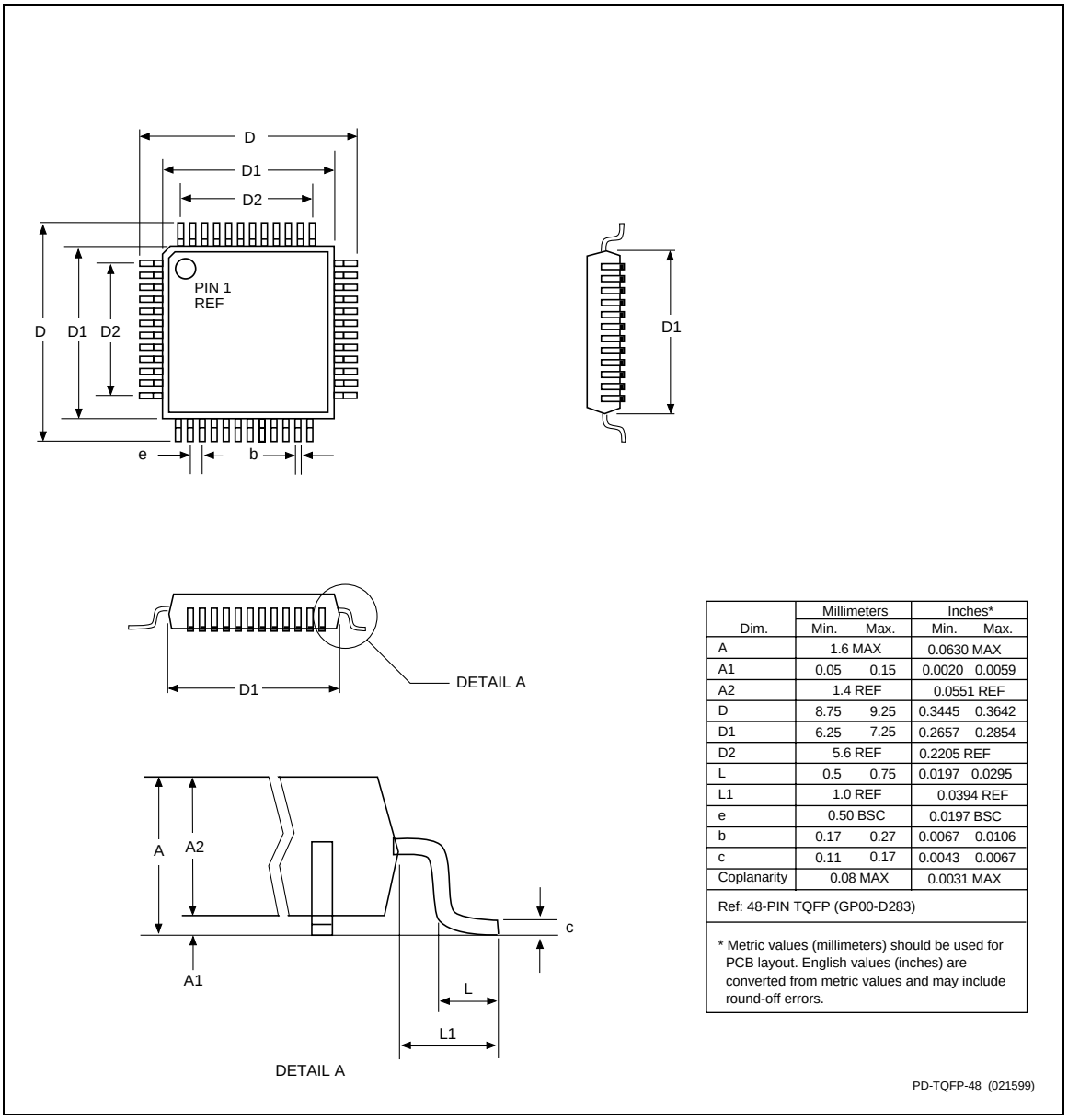
6 Package Dimensions

The package dimensions are shown in Figure 6-1 (48-pin TQFP) and Figure 6-2 (32-pin TQFP).

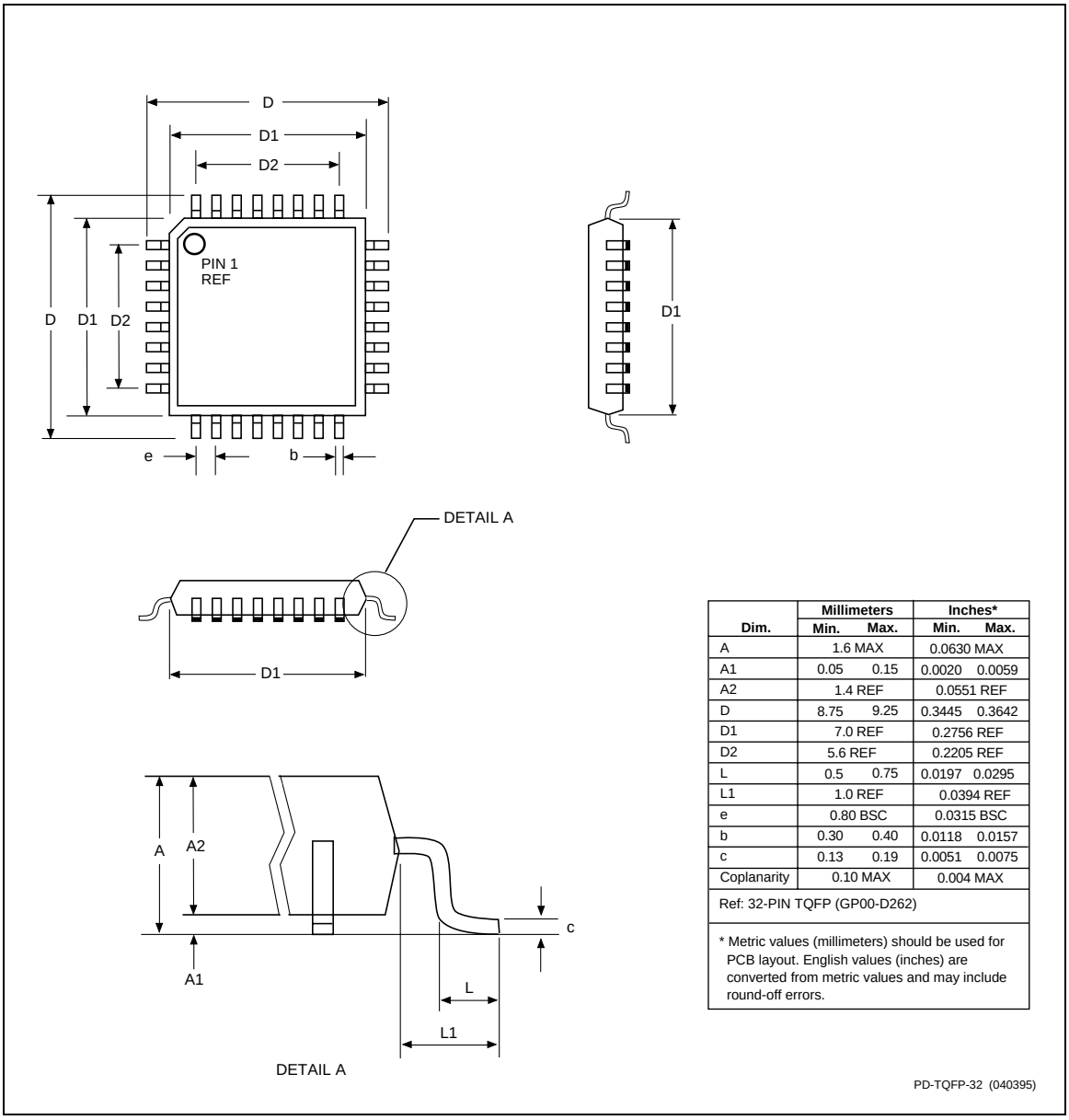


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	6.25	7.25	0.2657	0.2854
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

Ref: 48-PIN TQFP (GP00-D283)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 6-1. HSD Package Dimensions - 48-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 6-2. LSD Package Dimensions - 32-Pin TQFP

NOTES

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